TOMMASO RONCALLI

SIGMA
STEPPING MOTOR CONTROL MODULE SET

Part No. 29G01-21-41

APPLICATION BULLETIN MC-214

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SIGMA

CONTENTS

Section	Page
I. General Description of Modules	1.1 - 1.2
II. Ramp Control Logic Chip	2.1 - 2.8
III. Ramp Control Oscillator Chip	3.1 - 3.9
IV. Digital Motor Logic Circuit	4.1 - 4.9

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APPLICATION BULLETIN MC-214
STEPPING MOTOR CONTROL
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I. GENERAL DESCRIPTION OF MODULES

The Sigma Stepping Motor Control Chip Set consists of three separate MSI integrated circuits which may be used in a variety of ways to provide low-power signals for the control or actuation of stepping motor drive systems. The set is designed specifically to provide a compact hardware alternative to those control functions which require extensive hardware or software to duplicate. Further, those functions which often require adjustment, frequency and ramp slope, are performed in the analog domain to facilitate adjustment without reprogramming.

The circuits are constructed using bi-polar and CMOS circuitry, utilizing both linear and digital techniques. The set is designed to operate from a single 8-to-15 volt power supply. The input signals are typical logic levels, whereas most output signals are open-drain active circuits for maximum noise immunity.

Functionally, two circuits, the RCO and RCL chips, form a "buffered ramper" which provides a variable frequency pulse train to control the acceleration of a stepping motor from a fixed frequency burst of pulses. Pulses "lost" during acceleration are "recovered" during deceleration. Thus, smooth motor response is assured while the number of pulses is preserved.

Used alone, the RCO voltage-controlled oscillator and ramp generator can be used in a number of ways to generate fixed or variable frequency pulse trains, including ramped frequency trains for speed control applications.

The third circuit, the DML chip, accepts a pulse train and decodes it to stepping motor excitation formats: 2-3-4 phase, half-step, full-step, as well as providing for specialized damping schemes. This circuit is designed to be the heart of a motor winding power driver.

The three circuits of the set are categorized functionally as follows:

A. RCL Ramp Control Logic Circuit

The Ramp Control Logic IC is normally used in conjuction with the RCO circuit. The two circuits provide a method of providing a variable frequency pulse train to control the acceleration and deceleration of a stepping motor from a fixed frequency burst of pulses. The output of these chips can drive the DML Motor Logic IC or most any other stepping motor driver. The two IC's form a "Buffered Ramper". A buffered ramper accepts a constant high frequency pulse train and delivers a variable frequency output with preset acceleration and deceleration profiles.

B. RCO Ramp Control Oscillator

This linear bi-polar IC contains a precision VCO for V-to-F conversions, as well as highly stable, precision current sources for charging an external capacitor to generate stable symmetrical voltage ramps. These voltage ramps are used to generate ramped frequency outputs from the VCO section. This IC can be used in a number of ways in conjunction with stepping motors:

1. Phase-locked loop Buffered Ramper when used with the RCL IC.
2. VCO in phase-locked loop when used with other three-state phase detectors such as the Motorola MC 4046.
3. Fixed or variable frequency source for simple speed control.

4. Ramped frequency source for speed control from external control logic.
5. Parabolic response V-to-F converter ($F=KV^2$) for wide range frequency control, with or without ramping.

C. DML Motor Logic Circuit

This CMOS logic IC accepts a pulse train input and decodes it into a selectable, parallel output stepping motor phase excitation format. The IC is intended to be the heart of a motor driver, generating the output states required at Logic Power levels. Sufficient flexibility is present in the IC to fit most data input and output formats. The input can be either dual pulse trains, CW or CCW, or a pulse line and a direction line. The phase outputs can be two, three, or four phase in either the full-step or half-step sequences. In addition, the outputs can be in wave or overlapping sequences. Further, the phase outputs can be selectively disabled for either standby power reduction or damping. There are separate connections for a Reverse Pulse Damping input, and an Initial Reset input.

II. DESCRIPTION OF RCL CHIP: SIGMA PART NO. 29G01

A. General Description

The RCL Ramp Control Logic chip is a CMOS LSI circuit designed to operate in conjunction with the RCO IC to form a buffered ramper. This pair will accept a high speed, fixed frequency pulse train of length "N" and deliver a variable frequency pulse train of the same length with the acceleration and deceleration profiles required to operate stepping motor drive systems. The functional block diagram is shown in Figure 2.1.

The circuitry is housed in a 24-pin ceramic dual in-line package (Fig. 2.2). Although designed for 12 volts, it operates from a single positive 8-to-15 volt supply. The input lines are diode protected and internally terminated with pull-up loads to inter-connect with open collector signal sources. The outputs are low level totem pole drivers except for the phase comparator output. The phase comparator has a three state output designed especially to drive the RCO IC.

The circuit elements are CMOS gates and as such should be handled with the usual precautions and care reserved for CMOS circuits.

B. Detailed Description of Buffered Rampers

The Ramp Control Logic circuit, (RCL), is specifically designed to be used in conjunction with the Ramp Control Oscillator circuit, (RCO), to form a Buffered Ramper. As illustrated in Figures 2.3 and 2.4, there are two different cases of interest: Long-Pulse trains and Short-Pulse trains. In this discussion, a "Long" pulse train is defined as one which continues after the motor has accelerated fully to the maximum speed as shown in Fig. 2.3. A "Short" pulse train, Fig. 2.4, ends before the motor has reached final speed.

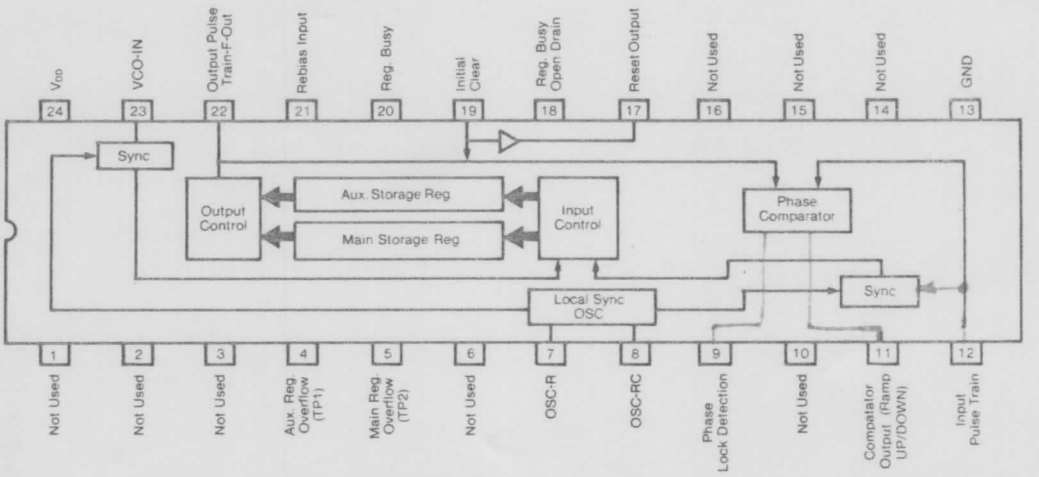


Fig. 2.1 Functional Block Diagram of RCL Module

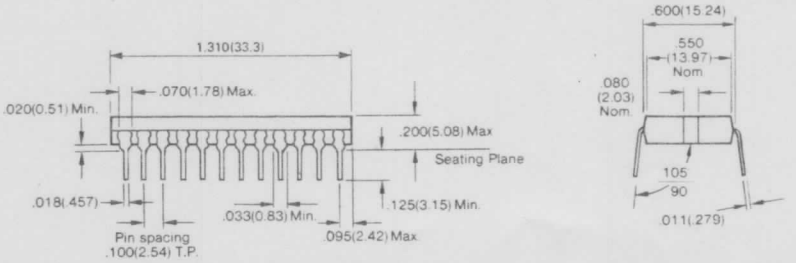


Fig. 2.2 Mechanical Outline Drawing for RCL Chip

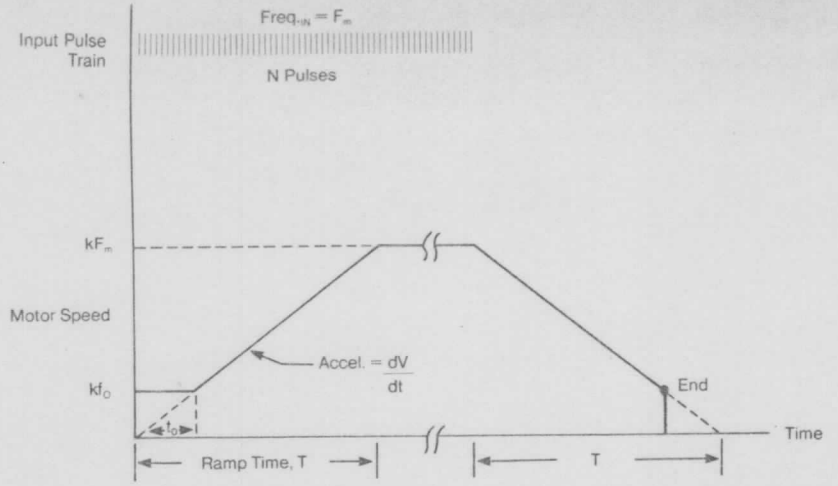


Fig. 2.3 Idealized Buffered Ramper Response to a Long Pulse Train

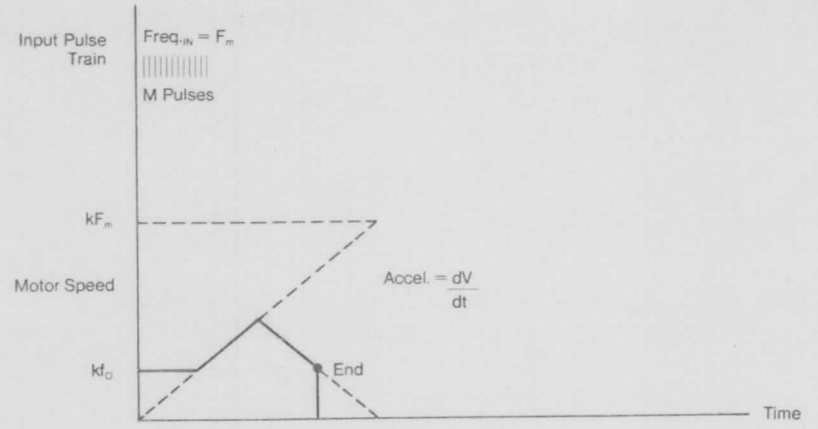


Fig. 2.4 Idealized Buffered Ramper Response to a Short Pulse Train

1. **Short Pulse Trains**

The Sigma RCL module contains specialized circuitry[1] which makes it particularly useful with short-pulse trains. In Fig. 2.4 the termination of the input pulse train does not cause the output frequency to decrease immediately as it does in the case of long-pulse trains, Fig. 2.3. The logic causes the output frequency to continue to increase until one-half of the number of input pulses has been delivered to the output. At this time, the output frequency is then caused to decrease. When the remaining half of the pulses are delivered, the output ends.

This response pattern assures the fastest response of the motor, considering an acceleration limit imposed by this system.

2. **Long Pulse Trains**

Referring to Fig. 2.3, the output frequency ramps up from some low frequency F_o, determined by the RCO circuit to the input frequency, F_m, in an acceleration period, T. When the output frequency reaches F_m, the Ramp Control Logic causes the Ramp Control Oscillator to phase lock on the input signal. As long as the input exists, the

[1]Patent applied for

output will be at F_m. When the input pulse train ceases, the output will decrease toward zero, ending at F_o.

During the acceleration period, T, the Ramp Control Logic stores the number of input pulses minus the number of output pulses. This number represents the number of pulses "lost" during acceleration, and must be recovered during deceleration. Accordingly, after the input pulse train ends, the output frequency decreases until the Main Register, containing the number of "lost" pulses, is counted back down to zero. At this time the output ends.

In Figures 2.3 and 2.4, the input pulse train is shown at a constant frequency, F_m. It is *not* a requirement that the input be constant. The input frequency can change after phase lock is reached as long as the rate of change is within the bandwith of the phase locked loop, i.e., within the bandwidth of the motor.

For short pulse trains, changes in F_{in} only affect the register counts, not the output pulse train. For long pulse trains, the limits on input frequency changes are two-fold:

a. After phase lock has been reached, the input must not change faster than the output can change, to avoid changes in the register counts.
b. The input frequency at the end of the pulse train must be at the same frequency that was present at the time phase lock was reached. Otherwise, the ramp down will not be symmetrical to the ramp up.

The register count must not exceed $16{,}000^+$ counts during acceleration, as described in the next section.

3. **Number of Input Pulses Stored**

During acceleration, the number of input pulses not delivered to the output are stored in a counter with a capacity of 16,383 pulses ($2^{14}-1$). In order to determine the storage capacity required, three cases must be considered. For simplicity, the input pulse train is assumed to be at a constant frequency, although it is not an exact requirement, as described previously.

a. **Very Short Pulse Trains**

In this case the input pulse train is complete before the output pulse train has accelerated above F_o. As shown in Fig. 2.4, if the input pulse train terminates before t_o, the output frequency is constant at F_o. Hence:

$$t \leq t_o$$

Number of Input Pulses = $F_m t$ Number of Output Pulses = $F_o t$

$$\therefore t = \frac{N_{in}}{F_m} \qquad \therefore N_o = F_o \times \frac{N_{in}}{F_m}$$

$$= \frac{F_o}{F_m} N_{in}$$

$$N_{stored} = N_{in} - N_{out}$$

$$N_{stored} = N_{in} - \frac{F_o}{F_m} N_{in}$$

$$N_{stored} = N_{in} \left(1 - \frac{F_o}{F_m} \right)$$

Thus, for large differences between F_m and F_o, the number of pulses stored approaches N_{in}. Therefore, N_{in} cannot exceed the register capacity of 16,000$^+$. In most systems, this limit will not even be approached.

b. Short Pulse Trains

In this case, the input pulse train terminates before phase lock with the input occurs, but after the output frequency has started to increase, Fig. 2.4. Hence:

Number of Input Pulses = $F_m t$ Number of Output Pulses = $\sum N_o$

$$\therefore t = \frac{N_{in}}{F_m} \qquad \sum N_o = \sum_{t=o}^{t=t_o} + \sum_{t=t_o}^{t=t}$$

$$N_{reg} = N_{in} - \sum N_o$$

$$N_{reg} = N_{in} - \frac{1}{2F_m T}[F_o^2 T^2 + N_{in}^2]$$

c. Long Pulse Trains

In this case, the input pulse train is sufficiently long so that phase lock between the input pulse train and the VCO output is achieved. Thus:

Number of Input Pulses = N_{in} Number of Output Pulses = $\sum N_o$

$$N_{in} = F_m T$$

$$N_{reg} = N_i - \sum N_o$$

$$\sum N_o = \frac{F_o^2 T}{F_m} + \frac{F_m T}{2}\left(1 - \frac{F_o^2}{F_m^2}\right)$$

$$N_{reg} = \frac{F_m^2 - F_o^2}{2F_m} T$$

Again, N_{reg} must not exceed 16,000$^+$, otherwise, data will be lost.

C. Detail RCL Circuit Operation

1. General:

Referring to the Block Diagram in Fig. 2.1, and the Connection Diagram in Fig. 2.5, the input pulse train is applied to pin 12 of the RCL IC. The input pulses should be positive going, with a width of at least 15 microseconds. At the output, the motor step is considered to occur on the trailing positive-to-negative transition. The frequency of the input pulse train must be equal to that required to produce the desired maximum motor speed. Since the VCO in the RCO chip will phase-lock to the input, the output of the buffered ramper will be equal to the input after acceleration is complete.

2. Logic Operation – Short Pulse Trains

The operation of the RCL circuit for short pulse trains is as follows. As soon as the first input pulse is received, these events occur:

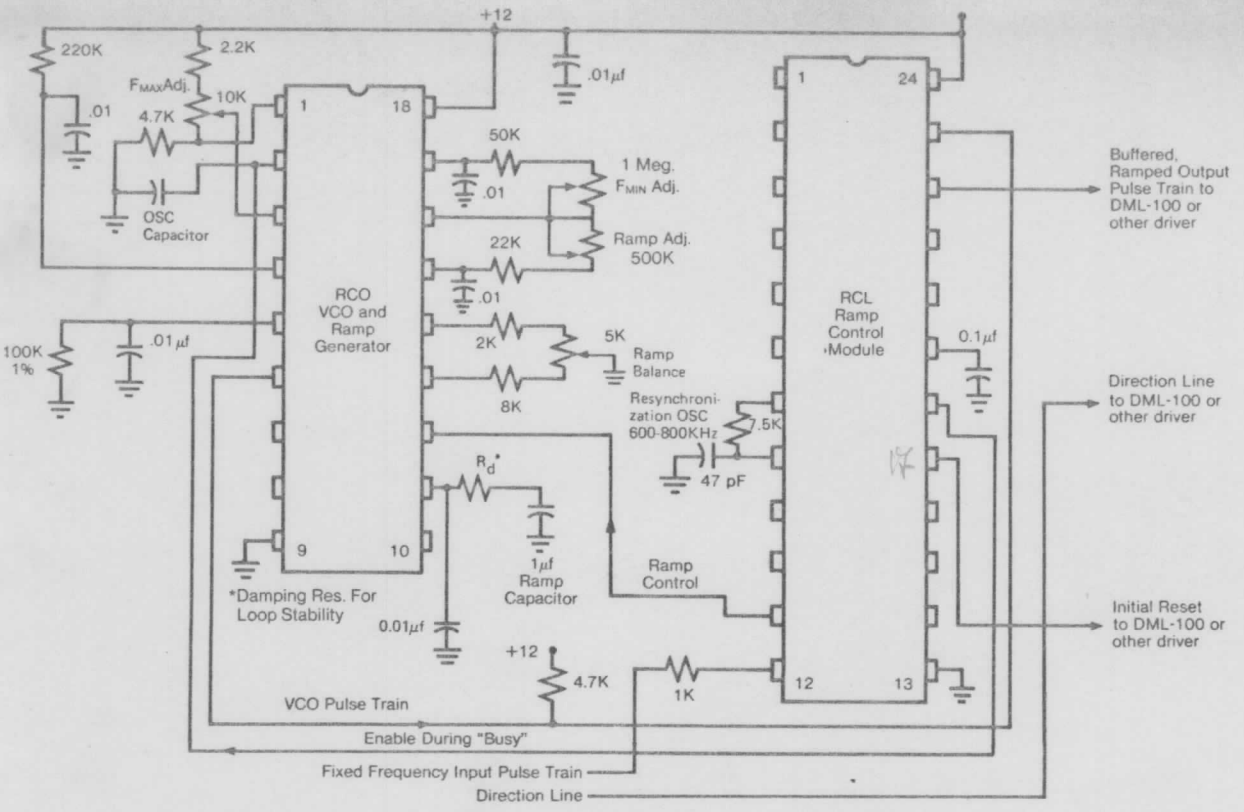


Fig. 2.5 Connection Diagram for Buffered Ramper

a. The RCL output line is enabled, pin 22.
b. The phase comparator output, pin 9, switches to logic 1 state, causing the RCO circuit to start a positive going ramp.
c. The Register Busy open-drain line, pin 18, releases the clamp on the oscillator capacitor, allowing the VCO to run.
d. The buffered Register Busy flag is set, putting a logic 0 on pin 20.

The RCO oscillator section output is applied to pin 23 of the RCL IC, and passes through to the output at pin 22. As the ramp voltage increases, the VCO output frequency increases.

There are two up-down counters used to keep track of the difference between the number of input and output pulses. The Main Register counts up on receipt of an input pulse, and counts down on an output pulse, storing the difference between the input pulses received and the output pulses delivered. The Auxiliary Register counts up in response to the input pulse train divided by 2, and counts down in response to the output pulse train. Thus, the Auxiliary Register returns to zero when one half the input pulses have been delivered to the output.

Accordingly, as shown in Fig. 2.6, as input pulses arrive, 14 in the example, the count in both registers increases. However, the Aux. Register reaches a maximum, then decreases to zero when the 7th pulse (½ the input number) appears at the output. It should be noted that even though the input pulse train ends, the output frequency continues to increase as long as the Auxiliary Register is not zero.

When the Aux. Register count goes to zero, and phase-lock is not reached, the internal logic enables the phase comparator output and causes the ramp control

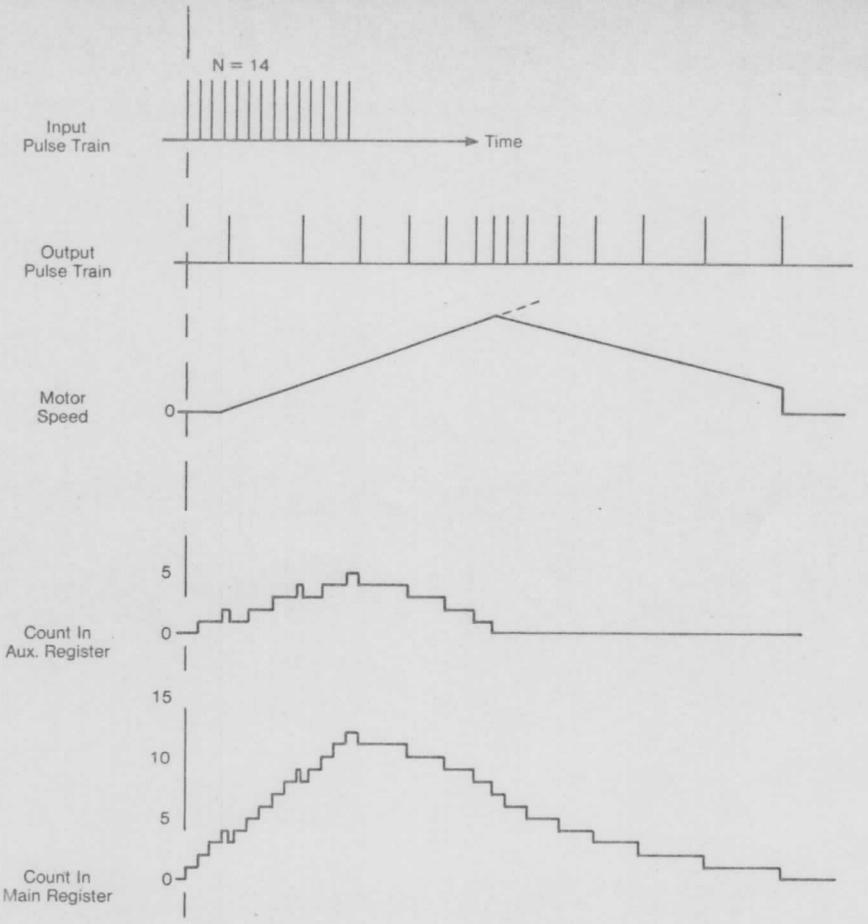


Fig. 2.6 Operation of Buffered Ramper for Short Pulse Trains

output, pin 11, to generate a decreasing VCO output; i.e. deceleration of the motor. When the Main Register goes to zero, all input pulses have been delivered. At this time, the Register Busy outputs reappear, the output gate is disabled, and the circuitry awaits a new input pulse train, and of course, the motor stops.

As described in the previous section, there is a limit of $2^{14}-1$ counts in the main register, and $2^{13}-1$ in the Aux. Register. The last stage of each counter is available on output pins of the RCL IC. Pin 5 is the last Main Register stage and pin 4 is the last Aux. Register stage. If a logic 1-0 transition is detected while the registers are busy, then an overflow has occurred and an error condition exists.

3. Logic Operation – Long Pulse Trains

The operation of the circuit for long pulse trains is very similar to that for short pulse trains, as shown in Fig. 2.7. The only difference occurs when the Auxiliary Register count goes to zero, the output frequency is very close to the input frequency and phase lock is achieved. The Phase Lock logic condition maintains the VCO at the input frequency and ignores the Aux. Reg. data. At the end of the input pulse train, the Phase Lock condition disappears and the VCO is commanded to ramp down. When the Main Register count goes to zero, the cycle ends as before.

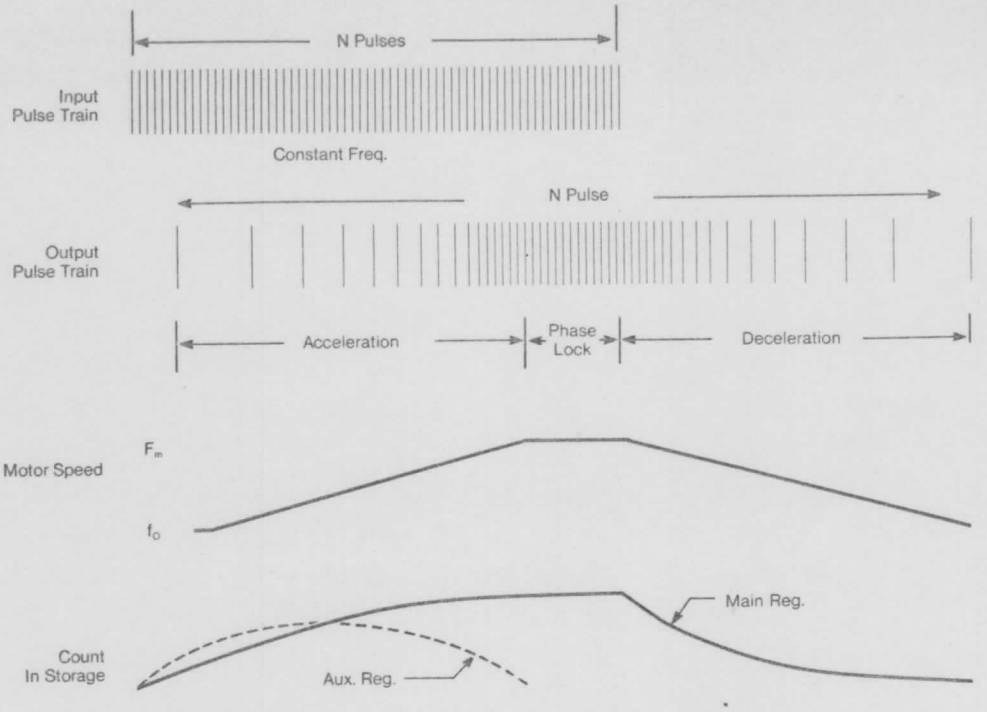


Fig. 2.7 Operation of Buffered Ramper for Long Pulse Trains

D. Description of Input and Output Signals

In the interest of circuit simplicity, especially when using open-collector input sources, all input lines are terminated internally with MOS pull-up current sources. These sources are generally sufficient to properly terminate an unused input requiring a logic 1 input. However, in those applications where unusually high noise may be encountered, termination of these lines to V_{DD} may result in higher noise immunity.

Input Lines	*Pin No.*	*Description*
F-in	12	System input: constant frequency. Pulse train at the frequency corresponding to the maximum desired motor speed.
VCO-in	23	Output from VCO section of RCO chip.
C	19	Clear input. A logic 0 resets all storage registers. A capacitor to GND on this line produces automatic reset during a Power On sequence.
OSC-R	7	Register R is part of frequency determining circuit for re-syncronizing oscillator. This oscillator frequency is not critical but should be between 600 KHz and 1 MHz.
OSC-RC	8	The junction of R, above, and a capacitor to GND.
F-out	22	Output pulse train. Equal in number to the input train, but variable in frequency (ramped) to accommodate acceleration characteristics of stepping motors. Totem pole output circuit.
Reg. Busy	20	Logic 1 indicates registers are empty, awaiting a new input pulse burst. Output is buffered with totem pole output.

Input Lines	*Pin No.*	*Description*
Reg. Busy	18	Same as pin 20 except has open drain buffer. Used to shunt down C_{osc} to disable VCO while waiting for an input.
RO	17	Reset output. Totem pole buffered signal identical to input on Pin 19. Used to reset motor driver, logic or DML Module.
CO	11	Phase comparator output. Used to control Ramp Section of RCO Chip. Logic 1 is ramp down. Logic 0 is ramp up. Has floating intermediate state (tri-state output).
PLD	9	Provides signal which indicates when phase-loop is in locked condition. Signal has an AC component and must be filtered.
TP1	4	Totem pole buffered output from Aux. Register. Logic 1 to 0 transition, (↓), indicates register has been overfilled and an error condition exists.
TP2	5	Totem pole buffered output from Main Register. A logic 1 to 0 transition, (↓), indicates register has been overfilled and an error condition exists.

TECHNICAL DATA–RATINGS AND CHARACTERISTICS

Maximum Ratings

Storage Temperature Range	−40 to +125°C	Supply Voltage V_{DD} to GND	16.5V
Operating Temperature Range	0 to +85°C	Package Power Dissipation	400mw

Operating Conditions at 25°C

Characteristic	Nominal	Min.	Max.	Units	
V_{DD}	12	8	15	V	± 10%
Supply Current	V_{DD} = 10V V_{DD} = 15V		0.5 1.0	mA	Built-in pull-up loads Logic inputs at GND
Input signal Voltage Range	0 to V_{DD}	$0.2V_{DD}$ to $0.8V_{DD}$	− 0.5V to V_{DD} + 0.5V	V	
Input Pulse Train Frequency			30	KHz	F_{IN} set to freq. equivalent to max. desired speed of motor.
Pulse width		15		μS	
Reset Pulse width		5		μS	
VCO Pulse Width		1.5		μS	
Freq. Re-Sync OSC	750	600	1000	KHz	Depends on Ext. R-C value

Static Electrical Conditions at 25°C

Characteristic	V_{DD}	Conditions	Min.	Nominal	Max.	Units	Pins
Logic input Current	10 15	Inputs at Logic 0 (GND)		10 10		pA pA	F_{in} RC
Logic input Current	10 15	Inputs at Logic 0 (GND)		0.16 0.35	0.3 0.5	mA	F_{VCO}
Logic input Current	10 15	Inputs at Logic 0 (GND)		8 15	15 30	μA	C
Logic input Current		Inputs at Logic 1 (V_{DD})		10pA		pA	F_{IN}, F_{VCO} etc.
Buffered Logic output Current Sink rating	10 15	V_{SAT} =0.5V	10 1.5			mA	Comp Out F_{out}, R_o etc.
Open Drain Busy output Current Sink	10 15	Output Logic 0 V_{SAT} = 0.5V	1.0 1.5			mA	
Open Drain Busy Voltage Rating		Output at Logic 1 V_S = 20V			10	μA	V_S = 20V Max.
Buffered Logic output Current Source	10 15	$V_{OUT} = V_{DD} - 1V$	1.0 1.5			mA	

III. DESCRIPTION OF RCO CHIP: SIGMA PART NO. 29G21

A. General Description

The RCO Ramp Control Oscillator Chip is an integrated bi-polar analog circuit designed to be used as a variable frequency pulse source for stepping motor drive systems. Although designed primarily for use in conjuction with the RCL ramper logic Chip, the device can be used to provide accurate and stable linear and parabolic V-F conversions, stable phase-locked loops, as well as linear frequency ramps. The device is particularly well suited to generate controlled acceleration and deceleration profiles for stepping motors. The circuitry is housed in an 18-pin ceramic dual in-line package (DIP) as shown in Fig. 3.2. It operates from a single 8-to-15 volt positive power supply, requiring less than 2 mA.

Referring to the Block Diagram of Fig. 3.1, the RCO module consists of four minor and two major circuits:

a) Temperature compensating Bias source.

b) Temperature compensated zener voltage source.

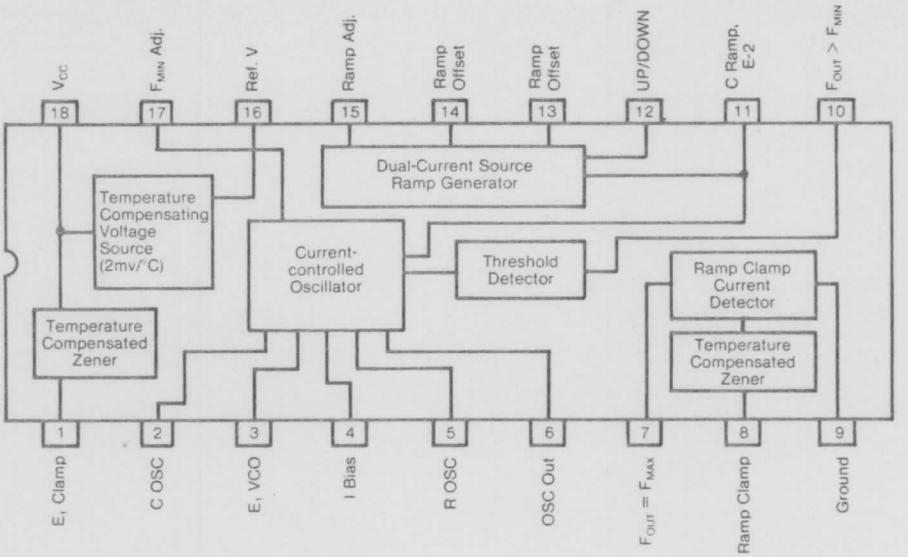


Fig. 3.1 Functional Block Diagram of RCO Chip

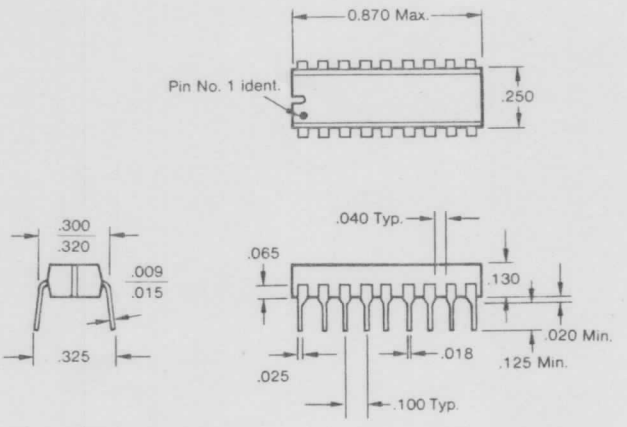


Fig. 3.2 Mechanical Outline Drawing for RCO Chip

c) Temperature compensated zener clamping diodes.
d) Amplifier saturation detector – $f > f_{min}$.
e) Oscillator voltage-to-current Converter and Threshold Comparator.
f) Ramp generator current sources.

B. Temperature Compensating Bias Source

The most important of the minor circuits is the temperature compensating voltage source whose output appears on pin 16. This source is used to generate two bias currents, set by means of external resistors, which provide adjustments of the ramp time, and the minimum output frequency, F_o. This source has a temperature coefficient equal but opposite to the temperature coefficients of a transistor base-emitter junction, about +2mV/°C.

C. Temperature Compensated Voltage Source

The second minor circuit is a temperature compensated zener diode connected between V_{cc} and pin 1. This diode has a voltage of about 7.2V ± 5%. It is used to generate a stable value for E1 (pin 3) when the module is used as a ramper. This diode need not be used if frequency stability is not required or, if V_{cc} is well regulated. The value of E1 to ground is not as important as the value of (V_{cc} – E1), hence the zener is between V_{cc} and pin 1. This allows the generation of a stable voltage relative to V_{cc}.

D. Compensated Ramp Clamp

The third minor circuit is a temperature compensated zener diode connected to ground. It also has a rating of 7.2V ± 5%. This diode is associated with circuitry to detect when the diode is conducting current. The usual use for this circuit is to clamp the input of the ramp capacitor voltage, pin 11, when the module is being used as a frequency source, and not under control of the Ramp Control Module.

This clamp serves two functions. First, it sets a stable upper limit to F_m when ramping (or other voltage control on pin 11). Second, it provides an output on pin 7 when the zener is conducting. This implies that f is equal to F_{max} because the input at pin 11 is clamped at a value limited by the zener diode.

E. Amplifier Saturation Detection

This circuit examines the condition of the V-to-I amplifier in the Oscillator section. If the V-to-I amplifier is in saturation, it is only because the bias current from an external adjustment for F_o (pin 17) is higher than the current required by the conversion of the ramp voltage on pin 11. If this is the case, then f_{out} is less than F_o. At this point, pin 10 is driven to ground. The threshold is not sharp, however. Thus, the open collector output is not accurate for load currents in excess of 3μa.

F. Oscillator Operation

The oscillator section consists of a voltage-to-current converter which produces a bipolar current proportional to the voltage on pin 11, E2 (Ramp Capacitor), the high impedance input of the V-to-I converter. Under the control of the threshold comparator, this current causes the external oscillator capacitor to charge or discharge linearly. Increasing E2 increases the current which increases the operating frequency.

The switching threshold of the comparator is established by applying a voltage, E1, at pin 3. By varying E1, the frequency changes; increasing E1 increases F. Thus, the output frequency can be controlled by either E1, a low impedance port (20-40K ohms), or by E2, a high impedance port (several megohms). The impedance level at E2, pin 11, was made high so that it could be driven from the ramp capacitor. In ramping operations, the external ramping current sources are connected internally to pin 11. *For non-ramping*

V-to-F conversions, pin 12, Ramp Control, must be allowed to float, disabling the ramp current sources. Otherwise, the ramp current sources may introduce undesirable effects if E2 is not driven from a low impedance voltage source.

Independent adjustments for F_{max} and F_{min} can be made easily. The temperature compensating voltage source on pin 16 is available to supply a small bias current to pin 17. This current limits the minimum value of the oscillator current when E2 approaches ground. Figure 3.3 shows the value of the ratio of F_o to F_m versus resistance between pins 16 and 17.

The maximum frequency is adjusted by varying the value of E1 (pin 3). The comparator thresholds are related to the difference between V_{cc} and E1. For this reason, the data in Figure 3.4 and 3.5 are given in terms of V_{cc} – E1. Thus, by adjusting E1 when E2 is at its maximum desired operating point, F_m can be set independently of F_o.

Figures 3.4 and 3.5 show the frequency relationship between E1 and E2 for linear V-F conversions. Figure 3.6 shows the output frequency as a parabolic function of V_{in}. These relationships hold for a wide range of capacitors (several decades) as long as the capacitor leakage is low ($\leq 0.1\mu a$) and the output frequency is less than 200 KHz.

The output of the oscillator is an open collector transistor, driven by the threshold

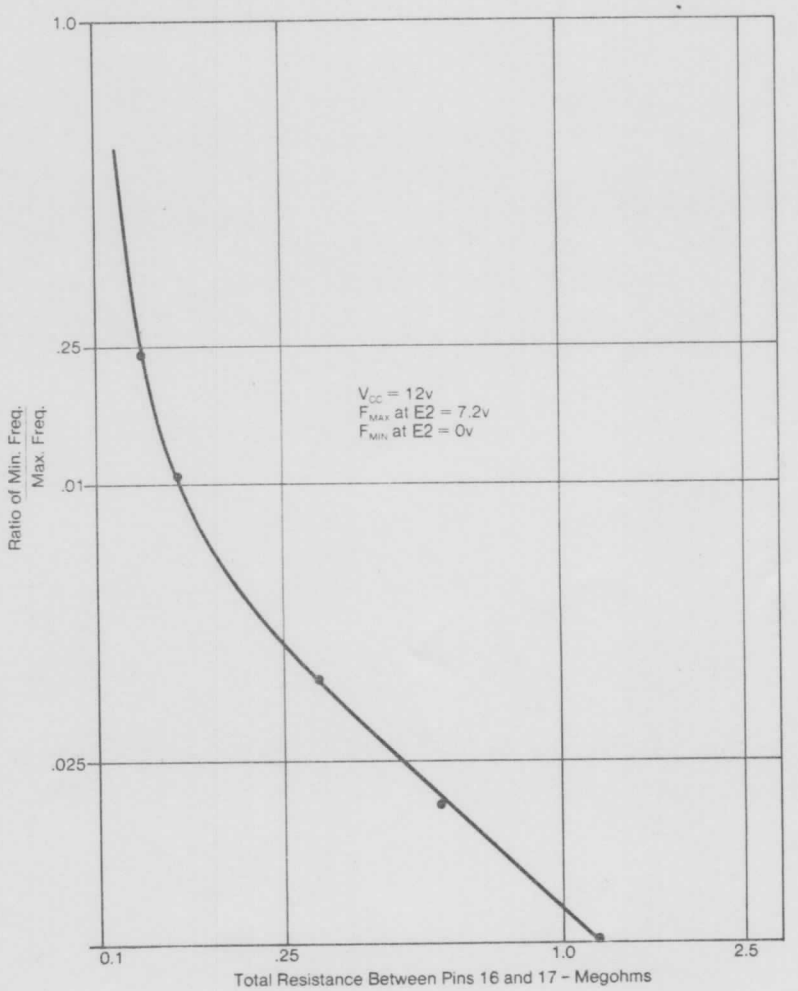


Fig. 3.3 Typical $\frac{F_o}{F_m}$ Versus Bias Resistance

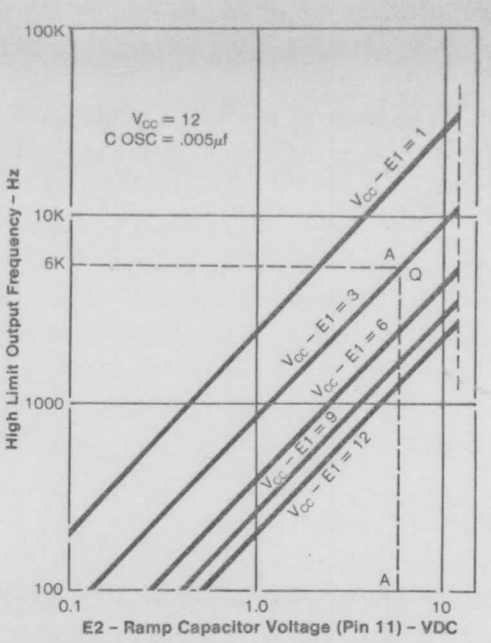


Fig. 3.4 Oscillator Frequency Range

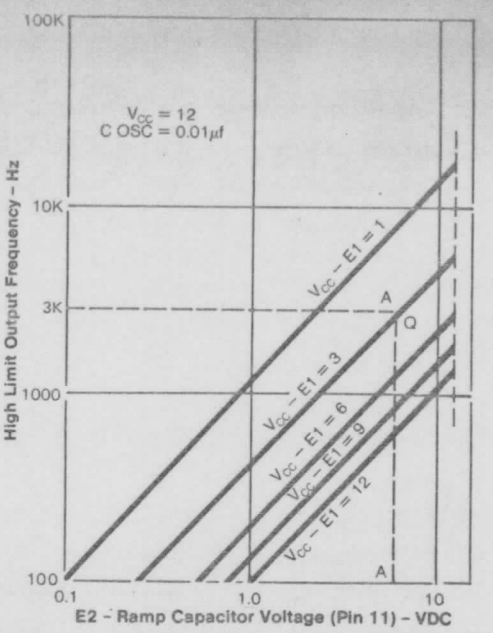


Fig. 3.5 Oscillator Frequency Range

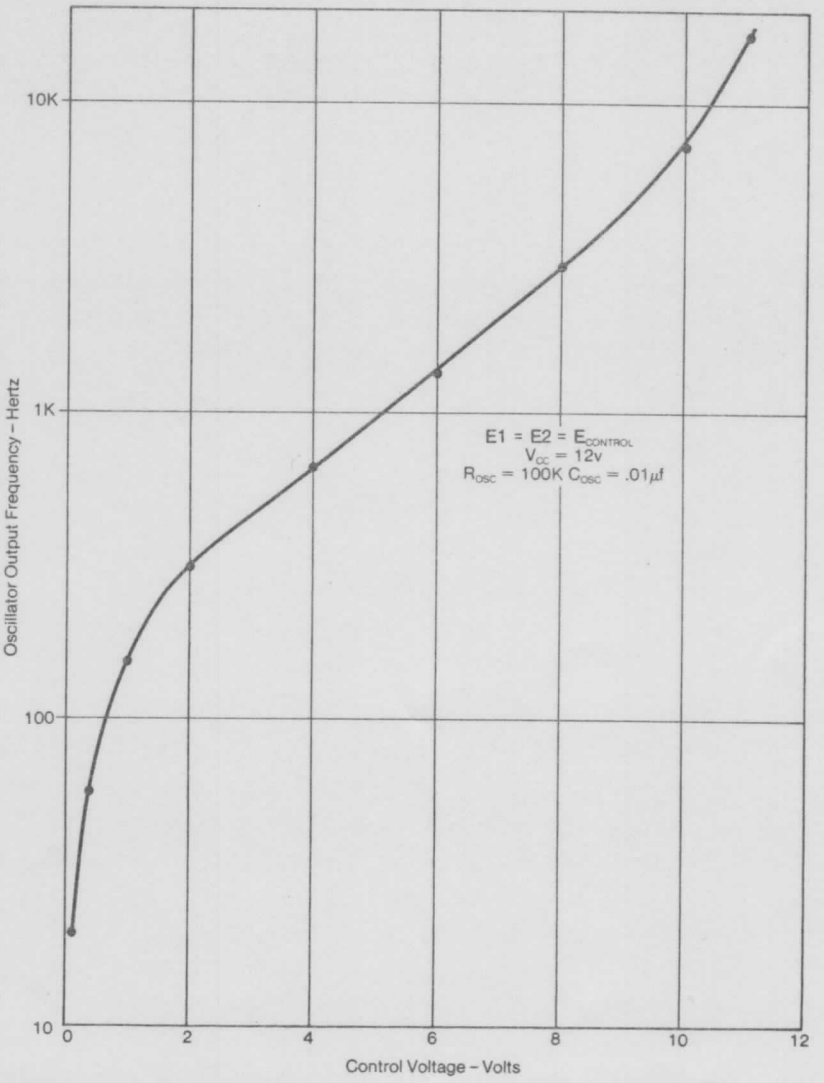


Fig. 3.6 Typical Parabolic Frequency-to-Voltage Conversion Response

comparator. Thus, with a resistive termination to V_{cc}, the output is a square wave at the operating frequency, with a duty cycle very close to 50%. The transistor is capable of sinking two to four T^2L loads, depending on the value of V_{cc}, and has a voltage rating of 20v minimum.

As noted previously, increasing either E1 or E2 increases the output frequency of the oscillator. Accordingly, if both E1 and E2 are driven from the same voltage source, F, the output frequency is almost a square law function of the input voltage ($F=kV^2$). Further, the range of the oscillator is very wide, more than 4 decades of frequency.

G. Ramp Generator

The ramp generator consists of two equal but opposite switched current sources. One source charges the external Ramp Capacitor toward V_{cc}, the other discharges it. The current sources are controlled by the voltage on the Ramp Control input, pin 12. This input accepts tri-state logic states. Applying V_{cc} to pin 12 causes the ramp voltage on pin 11 to increase toward V_{cc}. A ground voltage on pin 12 causes the ramp voltage to decrease toward ground. When pin 12 is floating, both current generators are switched off, allowing pin 11 to be used as an input to the VCO, or allowing the ramp capacitor voltage to remain fixed. In the floating configuration, the leakage currents are less than 1% of normal ramp currents. In most buffered ramping applications dealing with pulse trains of particular length, it is important that the Up-Ramp be symmetrical to the Down-Ramp, to avoid counting out the main accumulator at F_o or ending at a frequency higher than F_o. The ramp generator current sources can be balanced by inserting a balance potentiometer between pins 13 and 14. The pot can be omitted, and pins 13 and 14 grounded directly if desired. The slope of the ramp is determined by the Ramp Capacitor and by the current injected into pin 15, Ramp Adjust. The actual ramp time depends on the slope and the value of E2 selected. The choice of E2 is arbitrary. The ramp capacitor should be selected so that the resulting E2 is between 0.1 V_{cc} and 0.9 V_{cc}. Figure 3.8 shows the duration of 0 to 7.2 volt ramp as a function of the resistance between pins 15 and 16. The ramp time is closely proportional to C over several orders of magnitude. It is also closely proportional to magnitude of the ramp voltage, referred to ground.

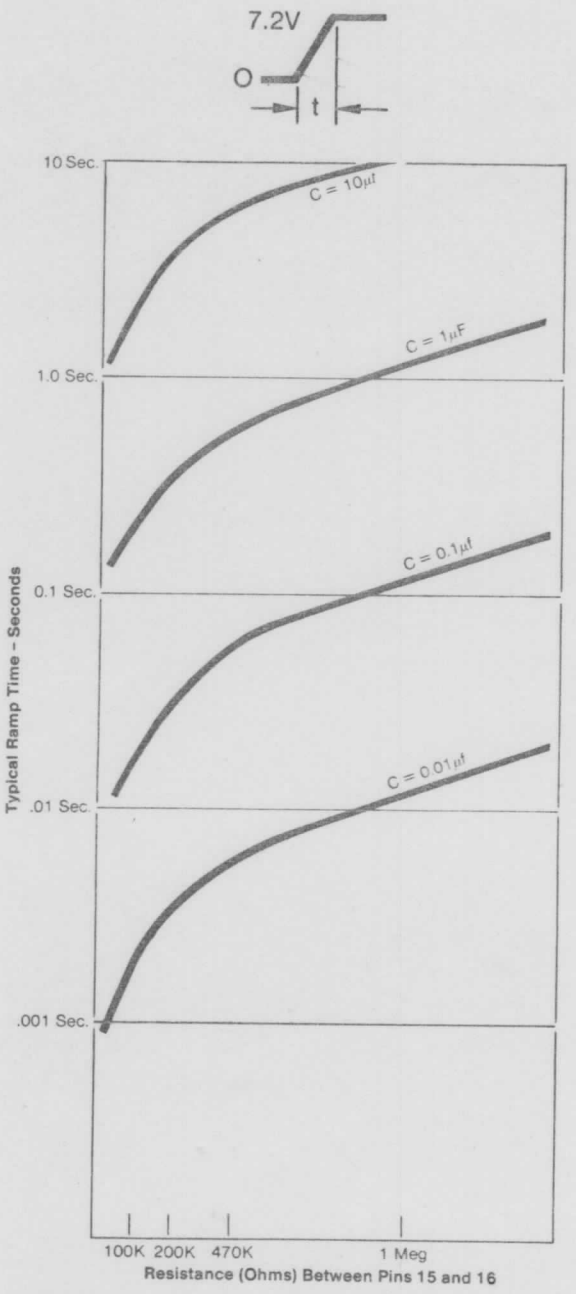


Fig. 3.8 Ramp Time (t) vs. Resistance

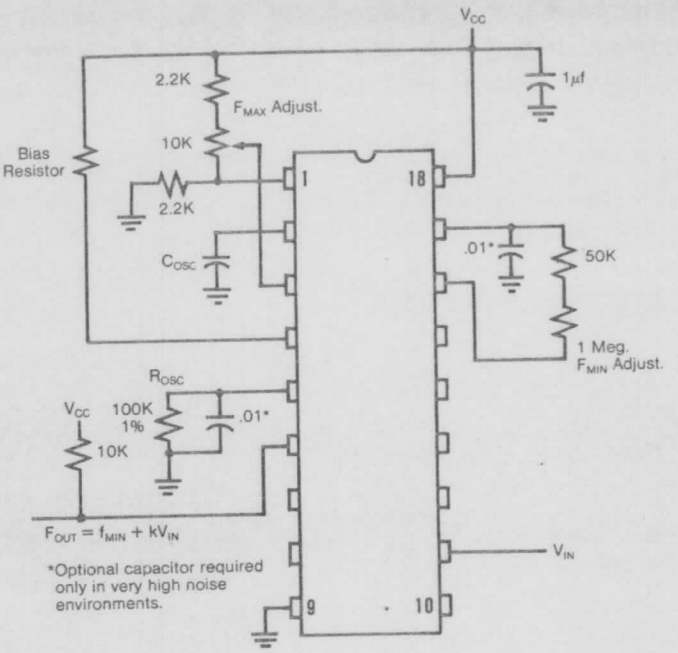


Fig. 3.7 Wide Range VCO with Linear Transfer Characteristics

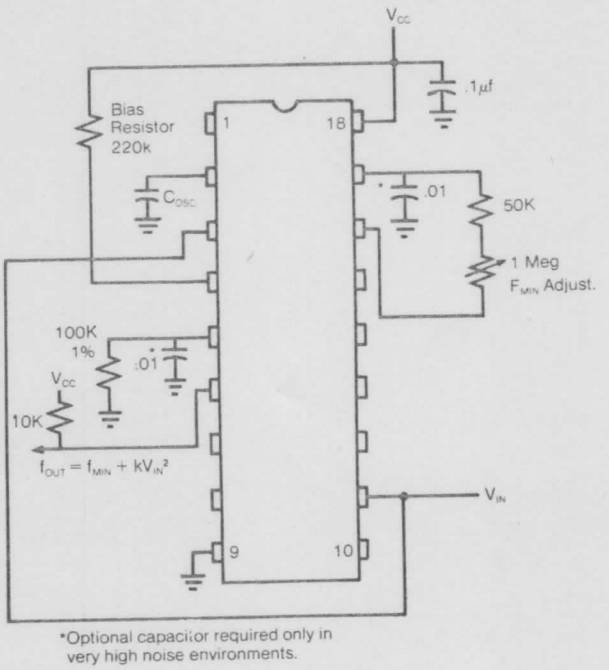


Fig. 3.9 Wide Range VCO with Parabolic Transfer Characteristics

H. Choice of Operating Point

There is a large degree of flexibility in the choice of operating points of the RCO circuits.

The ramp capacitor can be determined from Fig. 3.8. Assume arbitrarily that the bias resistor between pins 15 and 16 is 680K ohm, and that the ramp signal swings between zero and 7.2 volts, 60% to 70% of the power supply. Accordingly, the capacitor required can be determined. The exact ramp value can be adjusted by varying the bias resistor; however, in a Buffered Ramper or other Phase Locked Loop (PLL) application, variations of more than 10% in the bias resistors may seriously degrade the loop response dynamics and should be avoided.

The choice of threshold voltage is also arbitrary. A value of 3 volts less than the supply voltage, more or less, is a reasonable choice. Therefore, by way of example, in Fig. 3.5, a line AA is drawn from E2 equal to 7.2 volts which intersects the locus of $V_{cc}-E1=3$ at point Q. Extending a horizontal line to the frequency axis indicates that the operating frequency for F_m with an 0.01 μf capacitor will be about 3000 Hz. As indicated in Fig. 3.4, the operating frequency is inversely proportional to the oscillator capacitance, C_{osc}; therefore, the capacitor can be calculated for the desired operating point. Fine adjustment can be made by varying the threshold voltage, E1, on pin 3.

Therefore, to recap the procedure, the following comments apply:

1. Arbitrarily, pick ramp voltage E2 to swing between zero and 7.2 volts (10-15 volt power supply).
2. Pick C_{ramp} from Fig. 3.8, using 680K bias resistor. A fine adjustment of $\pm 10\%$ can be had by varying the bias resistor. Too much variation can upset loop dynamics.
3. Calculate C_{osc} from Figures 3.4 or 3.5 by using $E1=V_{cc}-3$ (arbitrary) and E2=7.2 volts. Adjust frequency by varying E1. This does not grossly effect loop dynamics.
4. Increasing E1 or E2 raises F_m. Decreasing C_{osc} raises F_m.
5. Set F_o by adjusting the bias resistor between pins 16 and 17, as indicated in Fig. 3.3.
6. Select the "damping" resistor in series with C_{ramp} as shown in Fig. 2.5 to provide the dynamic response required when the loop locks. A value between 3K ohms and 5K ohms is a good "First Try" value.

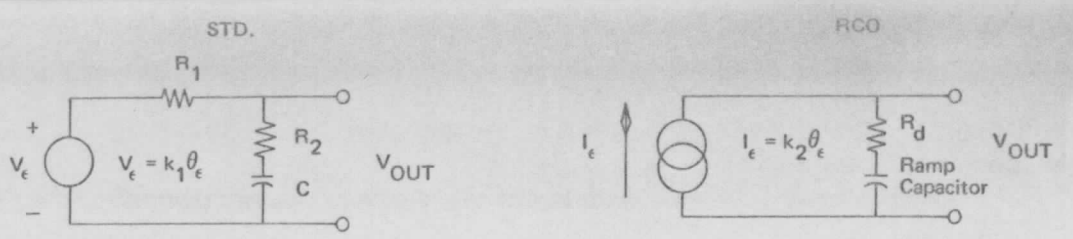
I. Stability of Phase Locked Loops

The PLL, created when the RCO and RCL circuits are used as a buffered ramper, constitute a servomechanism with a second order response.

Therefore, the transient response at the moment of capture can range from underdamped, characterized by large over-shoots and oscillatory decay, to a steady-state condition, to an over-damped response, slow but stable.

As shown in Figure 2.5, a resistor, R_d, is added in series with the ramp capacitor, connected to pin 11 of the RCO IC. This resistor value can be adjusted to provide the transient response required from the phase locked loop. In general, the smaller the resistor value, the more the output frequency over-shoot will be, and the wider and faster the capture range will be.

The choice of location of the resistor is based on the following: The VCO in the RCO circuit and the phase detector in the RCL circuit are easily recognized as elements of a conventional PLL. However, the ramp generator *current sources* and the ramp capacitor of the RCO perform the *same function* as the usual phase detector output filter. One form of the usual filter, driven from a voltage source, is:



The RCO circuit produces an equivalent filtering action, where I_ϵ is an increasing function of the phase error.

As noted before, a value for R_d ranges between 1K ohms and 10K ohms for most stepping motor requirements. The value is not particularly critical in most applications. This value is affected by the choice of the ramp bias resistor, since the bias resistor affects the loop gain by changing the current per radian of error angle. It is also affected by the ramp capacitor value.

An analysis of phase locked loops is beyond the scope of this bulletin; however, an excellent analysis of PLL's is given in:

Phaselock Techniques
Floyd M. Gardner
John Wiley & Sons, Inc.
New York, NY
1966
Library of Congress 66-22837

The only note of caution is that the phase detector output of the RCO chip is a *current* linearly proportional to the phase error, determined by the bias resistor between pins 16 and 15 of the RCO circuit. Obviously, adding a resistor in series with a current source (R_1) is not a change in loop dynamics; the whole loop analysis must be considered from the point of view of current sources, rather than voltage sources. None the less, the same philosophy applies to damping, response and capture bandwith.

J. Description of Input and Output Connections

Input Connections	*Pin No.*	*Description*
C-OSC	2	Basic frequency – determining element at oscillator section. Capacitor should be low-loss and temperature stable. See Figs. 3.4 and 3.5 for values.
E1-VCO	3	Sets thresholds of oscillator comparator. Increasing E1 increases frequency output. Normally used to set F_m when E2 is close to maximum desired operating point. Can be used as input for linear or parabolic V-to-F Conversions. The voltage between this point and V_{cc} is the value of interest for accurate prediction of output frequency.
I-bias	4	Sets bias currents for oscillator circuits. Normally connected to V_{cc} through a 220K resistor.
R-OSC	5	Sets currents for oscillator capacitor charging circuits. Normally connected to GND and by-passed with a small capacitor. Stable value of 100K is adequate for most systems.
Ramp Clamp	8	Zener diode to GND: normally connected to Ramp Capacitor input (pin 11), when module is used as ramper. Not used for externally controlled ramp, or when VCO is used for V-to-F conversions.

Input Connections	*Pin No.*	*Description*
C-Ramp	11	Voltage to frequency input, E2, connection for Ramp Capacitors. Capacitor should be low loss and stable. This input (as is E1-VCO) is a voltage input to the VCO. When not used for ramping, this high impedance input can be used for V-to-F conversions. An input here, or on E1 produces linear V-to-F conversion. If this pin and E1-VCO are connected, the conversion is parabolic and has an extremely wide range of control.
Up/Down	12	Ramp Control input. V_{cc} level causes the ramp capacitor voltage to increase toward V_{cc}. GND level causes ramp to decrease toward zero volts. No input causes the ramp capacitor charging current source to go to zero. This allows the capacitor voltage to remain unchanged (within the effects of leakage currents). For non-ramping V-to-F conversions, this point is not connected, disabling the current sources driving this point.
Ramp Offset	13 & 14	Terminals to which a potentiometer is connected to allow accurate balancing of the charge and discharge currents at the ramp capacitor. This allows the slope of the ramp-up and ramp-down to be identical. This terminal is especially important in critical ramping applications. May be grounded.
Ramp Adj.	15	Varying the current into this point provides adjustment of ramp time.
Ref.	16	A temperature-compensating voltage source, with a TC of about -2 mV/°C. Used to develop adjustment currents for Ramp Adj. and F_o Adj.
F_o Adj.	17	Varying the current into this point adjusts the F_o frequency when the C-Ramp voltage, E2, is close to ground potential.
E1-Clamp	1	A temperature compensated Zener diode connected to V_{cc}. Allows generation of a stable E1 voltage when V_{cc} is not regulated. Used in critical ramping applications. See Fig. 3.7. Can also be used to generate stable E1 voltages for V-to-F conversions.
OSC-OUT	6	Open-drain oscillator output. Will sink 2 mA to GND. Requires external pull-up load.
$F_{out}=F_{max}$	7	A very high impedance current sink which operates only when the ramp clamp function is used. Produces active ON state when Ramp-Clamp draws current; i.e., when ramp reaches upper limit and $F_{out}=F_m$. Will not develop a sharp threshold for currents more than 15μa, although the sink capability is in excess of 1 mA.
$F_{out} > F_{min}$	10	A very high impedance current sink which can be used for monitoring functions. Produces active ON state when F_{out} is higher than the F_{min} value. Output will sink 3μa and still provide sharp thresholds.

IV. DIGITAL MOTOR LOGIC CIRCUIT DML: SIGMA PART NO. 29G041

A. General Description

The DML Digital Motor Logic IC is a CMOS MSI circuit designed to accept an input pulse train and decode it to a selectable, parallel output, stepping motor phase excitation format. The functional block diagram is shown in Fig. 4.1. The circuitry is housed in an 18-pin ceramic dual in-line package (Fig. 4.2). It operates from a single positive 8-to-15 volt power supply. Input lines are diode protected and internally terminated with pull-up current sources. The phase sequence outputs are open drain active circuits, rated at 10 mA for 12-volt systems, for maximum noise immunity and system performance. The circuit elements are CMOS gates and as such should be handled with the usual precautions and care reserved for CMOS circuits.

1. Pre-programmed Functions

The input and output data formats are pre-programmed to provide the following selectable functions:

Phase outputs – Three-phase.
Two-phase (also known as "four-phase")
Wave Drive
Overlapping (also known as "two-phase")
Full Step
Half Step

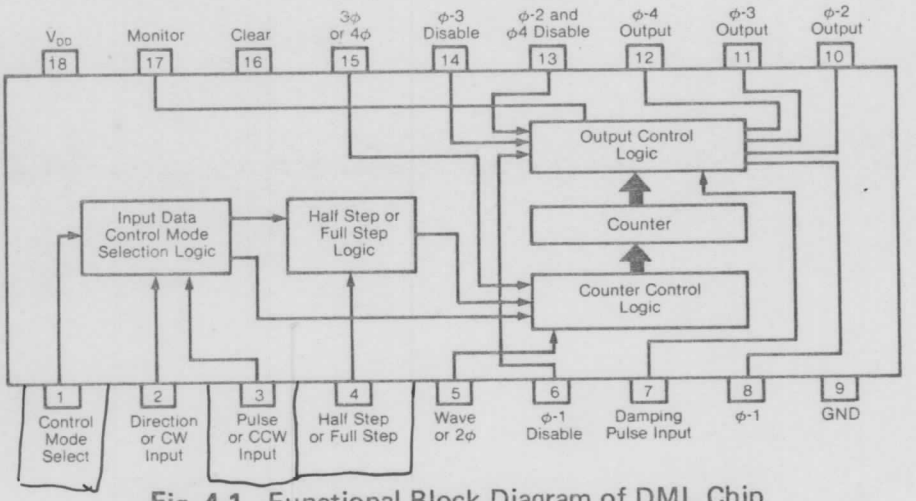


Fig. 4.1 Functional Block Diagram of DML Chip

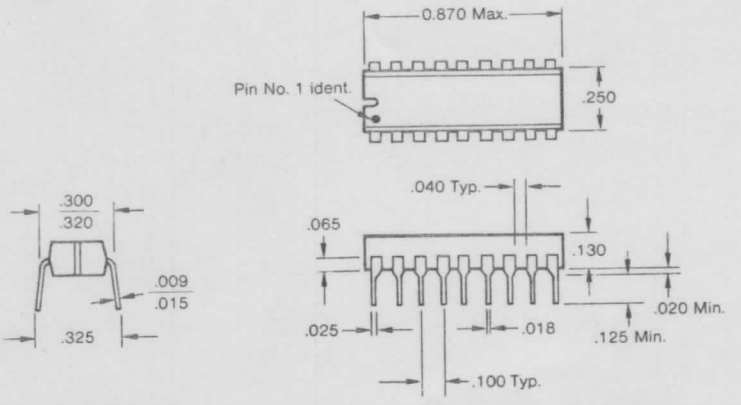


Fig. 4.2 Mechanical Outline Drawing for DML Chip

Input Data – Independent CW and CCW pulse trains.
Pulse train and Direction

The following inputs or outputs are available for system flexibility:

Initial reset input
Independent phase disable lines inputs
Initial-reset-state monitor output
Reverse pulse damping input.

B. Detail Description

The DML Digital Stepping Motor Logic IC is a general purpose MSI circuit designed to generate a set of low-power waveforms required to drive stepping motors. In addition, either of the two most common input data formats can be accepted.

Actual input motion data are received on two input lines. Output motion data are supplied on four output lines. The input data can be two independent but mutually exclusive pulse trains: one for CW motion and the other for CCW motion. An alternative input data format consists of a single pulse train, and a line carrying the directional information as a logic 0 or 1. The choice between these two formats is selectable as described in the following section, "Description of Input and Output Conditions". The output data can be selected to provide either two-phase or three-phase sequences. The term "two-phase" also includes the option for the sequence known as "four-phase". Technically, the four-phase sequence is a set of excitation sequences for a motor with two-phase, center tapped windings. See Truth Table One and Fig. 4.1 for the connections to produce this drive sequence. In addition to the conventional input and output connections, three inputs are available to disable the phase outputs. These can be used for a number of special purposes. These include:

1. **Reduction of stand-by motor power.**
   a. Disable one phase (one or two phase-disable lines)
   b. Disable all phases (all three phase-disable lines)
2. **Specialized damping**
   a. Reverse pulse damping input, DP
   b. Phase output disable inputs.
3. **Cross-over protection** (phase disable lines can be used to prevent line-to-line short circuits caused by transistor storage delays on full bridge drivers).

C. Description of Input and Output Functions

In the interest of circuit simplicity, especially when using open collector input sources, all input lines are terminated internally with MOS pull-up current sources. These sources are generally sufficient to properly terminate an unused input line requiring a logic 1 input. However, in those applications where unusually high noise may be encountered, termination of these lines to V_{dd} may result in higher noise immunity.

Input Functions	*Pin No.*	*Description*
2-phase or 3-phase	15	Logic 0 selects a 2-phase (also known as 4-phase) output sequence. Logic 1 selects for 3-phase output sequence. See Truth Table One for output sequences.
Wave or 2-phase	5	Logic 0 selects wave drive; i.e., only one output energized per state. Logic 1 selects "2-phase" (or "overlapping"), two outputs energized per state. See Truth Table One for output sequences.

Input Functions	*Pin No.*	*Description*
Full Step or Half Step	4	Logic 0 selects full step drive; i.e., continuous sequences in either wave drive or 2-phase drive. Logic 1 selects half-step drive which is a pattern which alternates successively between wave and 2-phase drive which results in a motor step which is one-half the size of that produced by either wave or overlapping drive. See Truth Table Two for output sequences. Selection of half-step overrides the selection of wave drive or 2-phase drive.
Control Mode Select	1	This input selects between two forms of input data and modifies the function of data appearing on pins 2 and 3. A logic 1 on this input conditions the input data logic to accept an input pulse train on either pin 2 for CW motion or on pin 3 for CCW motion. A logic 0 on pin 1 conditions the circuitry to accept a pulse train on pin 3 and a direction command [redacted] on pin 2. See Truth Table Three for input functions.
Direction or CW Input	2	If pin 1 is a logic 0, a pulse train on this pin will produce a CW rotational pattern on the output. The phase outputs will change on the transition from high to low of the input pulse train. If pin 1 is a logic 1, pin 2 accepts directional input data: 1=CW; 0=CCW. See Truth Table Three for description of states. See Fig. 4.3 for timing requirements.
Pulse Train on CCW Input	3	If pin 1 is a logic 0, a pulse train on this pin will produce a CCW rotational pattern on the output. The phase outputs will change on the transition from high to low of the input pulse train. If pin 1 is a logic 1, pin 3 also accepts an input pulse train; however, the direction is controlled by the signal on pin 2. The outputs change in response to the transition of the pulse train from high to low. See Truth Table Three.
Clear	16	A logic 0 on this pin resets the logic so that a logic 1 appears on phase 1 output for wave drive, or on phases 1 and 2 for 2-phase drive. See Truth Tables One and Two. This input can be used to provide an automatic reset during initial power on by connecting a capacitor between this pin and GND.
OD1	6	A logic 1 on this pin unconditionally forces a logic 0 on the phase 1 output.
OD2	13	A logic 1 on this pin unconditionally forces a logic 0 on phase 2 and phase 4 outputs.
OD3	14	A logic 1 on this pin unconditionally forces a logic 0 on the phase 3 output.

Input Functions	*Pin No.*	*Description*
DP	7	A logic 1 on this pin unconditionally causes the phase outputs to assume the output states present *just prior* to the last clock pulse. The effect is to cause the motor to reverse one step. It is intended to be used for reverse pulse damping.

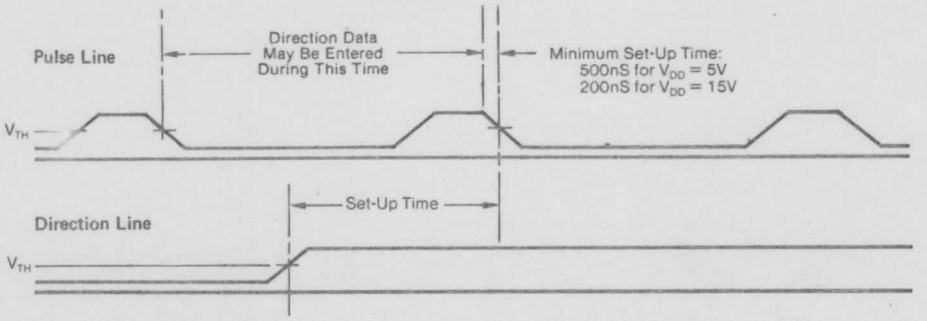


Fig. 4.3 Logic Module Direction Line Timing Requirements

Output Functions	*Pin No.*	*Description*
MON	17	This output is a logic 1 whenever the phase 1 output is a logic 1 wave drive, or when phases 1 and 2 are both at logic in 2-phase drive. This corresponds to the Initial Reset condition.
Ø1	8	Phase 1 output: See Truth Tables One and Two for sequences. The output transistor is conducting during a logic 0 output. A pull-up resistor must be provided.
Ø2	10	Phase 2 output: See Truth Tables One and Two for sequences. The output transistor is conducting during a logic 0 output. A pull-up resistor must be provided.
Ø3	11	Phase Three output: See Truth Tables One and Two for sequences. The output transistor is conducting during a logic 0 output. A pull-up resistor must be provided.
Ø4	12	Phase Four output: See Truth Tables One and Two for sequences. The output transistor is conducting during a logic 0 output. A pull-up resistor must be provided.

TRUTH TABLE ONE

FULL STEP OUTPUT STATES

Pin 1 = 0 Pin 4 = 0 Pin 7 = 0 Pins 6, 13, 14 = 0

				Pin 5 = 0				Pin 5 = 1				
c/r	3φ/4φ	Dir/cw	Pulse/ccw	φ4	φ3	φ2	φ1	φ4	φ3	φ2	φ1	MON.
O	X	X	X	O	O	O	I	O	O	I	I	I
Three Phase States												
I	I	I	↓	O	O	I	O	O	I	I	O	O
I	I	I	↓	O	I	O	O	O	I	O	I	O
I	I	I	↓	O	O	O	I	O	O	I	I	I
I	I	O	↓	O	I	O	O	O	I	O	I	O
I	I	O	↓	O	O	I	O	O	I	I	O	O
I	I	O	↓	O	O	O	I	O	O	I	I	I
Two Phase States												
I	O	I	↓	O	O	I	O	O	I	I	O+	O
I	O	I	↓	O	I	O	O	I	I	O	O+	O
I	O	I	↓	I	O	O	O	I	O	O	I+	O
I	O	I	↓	O	O	O	I	O	O	I	I+	
I	O	O	↓	I	O	O	O	I	O	O	I+	O
I	O	O	↓	O	I	O	O	I	I	O	O+	O
I	O	O	↓	O	O	I	O	O	I	I	O+	O
I	O	O	↓	O	O	Ø	I	O	O	I	I+	I

O = Low level I = High level ↓High-to-low transition X = Don't care

+These states are commonly referred to as two-phase or also as four-phase drive.
A four-phase motor is a center tapped two-phase motor.

TRUTH TABLE TWO

HALF STEP OUTPUT STATES

Pin 1 = 0 Pin 4 = 1 Pin 7 = 0 Pin 6, 13, 14 = 0 Pin 5 = X

c/r	3φ/4φ	Dir/cw	Pulse/ccw	φ4	φ3	φ2	φ1	MON.
O	X	X	X	O	O	O	I	I
Two Phase States								
I	O	I	↓	O	O	I	I	O
I	O	I	↓	O	O	I	O	O
I	O	I	↓	O	I	I	O	O
I	O	I	↓	O	I	O	O	O
I	O	I	↓	I	I	O	O	O
I	O	I	↓	I	O	O	O	O
I	O	I	↓	I	O	O	I	O
I	O	I	↓	O	O	O	I	I
I	O	O	↓	I	O	O	I	O
I	O	O	↓	I	O	O	O	O
I	O	O	↓	I	I	O	O	O
I	O	O	↓	O	I	O	O	O
I	O	O	↓	O	I	I	O	O
I	O	O	↓	O	O	I	O	O
I	O	O	↓	O	O	I	I	O
I	O	O	↓	O	O	O	I	I

c/r	3φ/4φ	Dir/cw	Pulse/ccw	φ4	φ3	φ2	φ1	MON.
O	X	X	X	O	O	O	I	I
Three Phase States								
I	I	I	↓	O	O	I	I	O
I	I	I	↓	O	O	I	O	O
I	I	I	↓	O	I	I	O	O
I	I	I	↓	O	I	O	O	O
I	I	I	↓	O	I	O	I	O
I	I	I	↓	O	O	O	I	I
I	I	O	↓	O	I	O	I	O
I	I	O	↓	O	I	I	O	O
I	I	O	↓	O	O	I	O	O
I	I	O	↓	O	O	I	I	O
I	I	O	↓	O	O	O	I	I

O = Low level I = High level
↓ = High-to-low transition X = Don't care

TRUTH TABLE THREE

INPUT DATA MODES

Function

	PIN 2	PIN 3
PIN 1 = 0 (pulse train and direction lines)	Direction input 1 = cw 0 = ccw See figure 14 for timing requirements relative to pulse train.	Pulse train input Pattern changes on high-to-low transition.
PIN 1 = 1 (cw pulse train and ccw pulse train)	Pulse train causes cw rotation, change occurs on high-to-low transition.	Pulse train causes ccw rotation, change occurs on high-to-low transition.

TECHNICAL DATA—RATINGS AND CHARACTERISTICS

Maximum Ratings

Storage temperature range	−40 to +125°C	Phase output current sink capability	50mA
Operating temperature range	0 to + 85°C	Total package power dissipation+	400mW
Supply voltage V_{DD} to GND	16.5V		

+ derate at 100°C/watt to max junction temperature of 125°C

Operating Conditions at 25°C

Characteristic	Nominal	Min.	Max.	Units	
V_{DD} range	12	5	15	V	± 10%
Input voltage range	0 to V_{DD}	$0.2V_{DD}$ to $0.8V_{DD}$	−0.5V to V_{DD} +0.5V	V	
Pulse freq.		DC	200	KHz	KHz
Pulse width		2.5	None	μS	
Reset pulse width		5	None	μS	
Damping P.W.		5	None	μS	Motor + Sys. Dependent
Phase Dis. P.W.		5	None	μS	Motor + Sys. Dependent
Damping pulse delay			50	μS	
Phase Dis. delay			50	μS	
Pulse input rise		None	10	μS	
Direction input Set-up time	V_{DD} = 5V V_{DD} = 15V	500 200	None None	μS μS	See Figure 4.3

Static Electrical Conditions at 25°C

Characteristic	V_{DD}		Min	Nom	Max	Units	
Static Device Supply Current	5V 10V 15V	All-inputs Logic 0 (GND)		4 10 20	5 15 30	mA	Built-in pull-up loads
Logic input current	5V 10V 15V	All inputs logic 0 (GND)		.4 1.1 2.0	.6 1.6 2.5	μA	
Logic input current		All inputs logic V_{DD}			±100	nA	
Phase output voltage rating		Logic 1 out	20	35		V	
Phase output leakage current		Vs=20V			10	μA	
Phase output current sink capability	5V 10V 15V	Vsat= 1.0V	5 10 15			mA	
MON. output current sink capability	5V 10V 15V	Vo=0.5V	0.40 0.81 1.2			mA	
MON. output current source capability	5V 10V 15V	Vo=VOD −I.D.	0.5 1.0 1.5			mA	

D. Operational Circuits

The DML IC is designed to provide logic level signals to a wide variety of phase winding drivers. Figures 4.4 through 4.8 show only a few of the possibilities possible. Figures 4.4 and 4.5 show simple two-phase and three-phase drivers. For more complex system requirements, two special inputs are available. A special input line is provided to generate the output conditions for reverse pulse damping. This damping scheme is used to improve the transient response of a stepping motor system. In a typical system, Fig. 4.8, a pulse of duration T_2, is applied to the DP input after a time delay of T_1. This, in effect, energizes the motor in such a way as to attempt to cause the motor rotor to rotate backward at the end of T_1, thus removing excess kinetic energy from the rotor and load during interval T_2. By proper choice of T_1 and T_2, the motor can be almost critically damped on the last step of a pulse train, or on every step if the input frequency is low enough.

A special output monitor line is provided, the MON line. This line can be used for checking or test purposes. MON goes to a logic 1 whenever phases 1 and 2 return to the logic condition generated by the initial reset. See Truth Tables One and Two. For example, it can be used to determine if an input pulse sequence has completed 4xN steps since the initial reset for two-phase motor. That is, the MON line goes to a logic 1 state every fourth pulse after a reset.

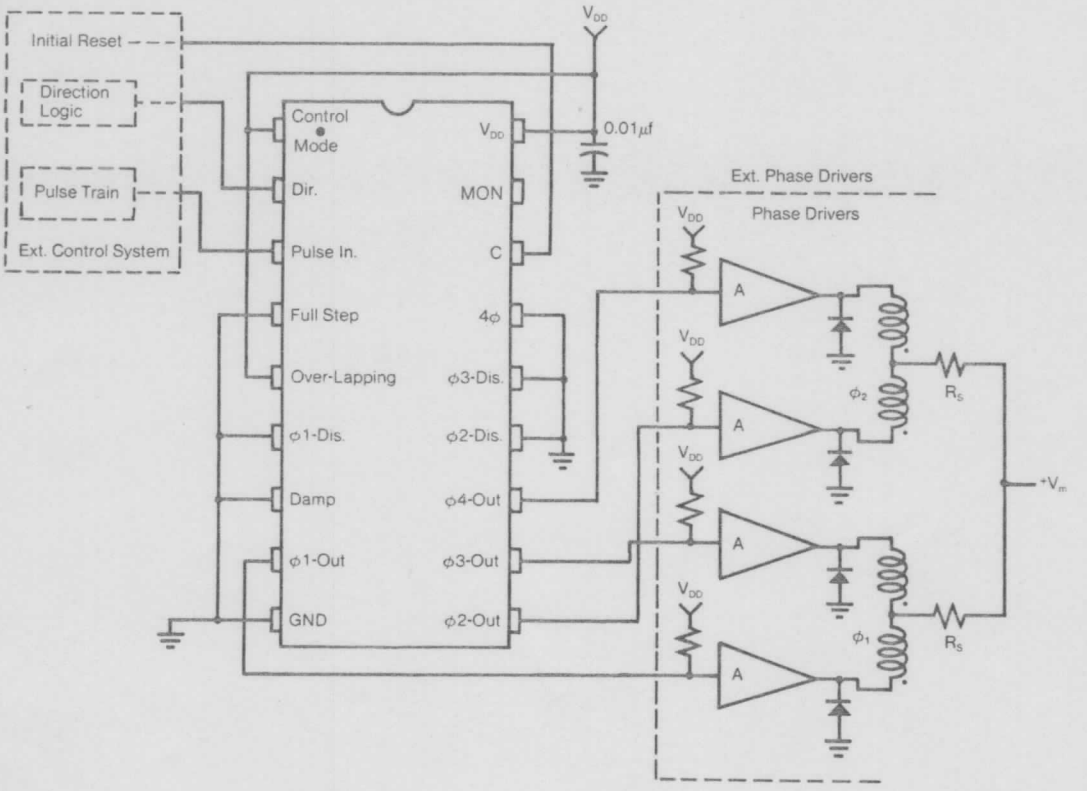


Fig. 4.4 Connections for Two-Phase, Full Step Driver with Two Windings Energized

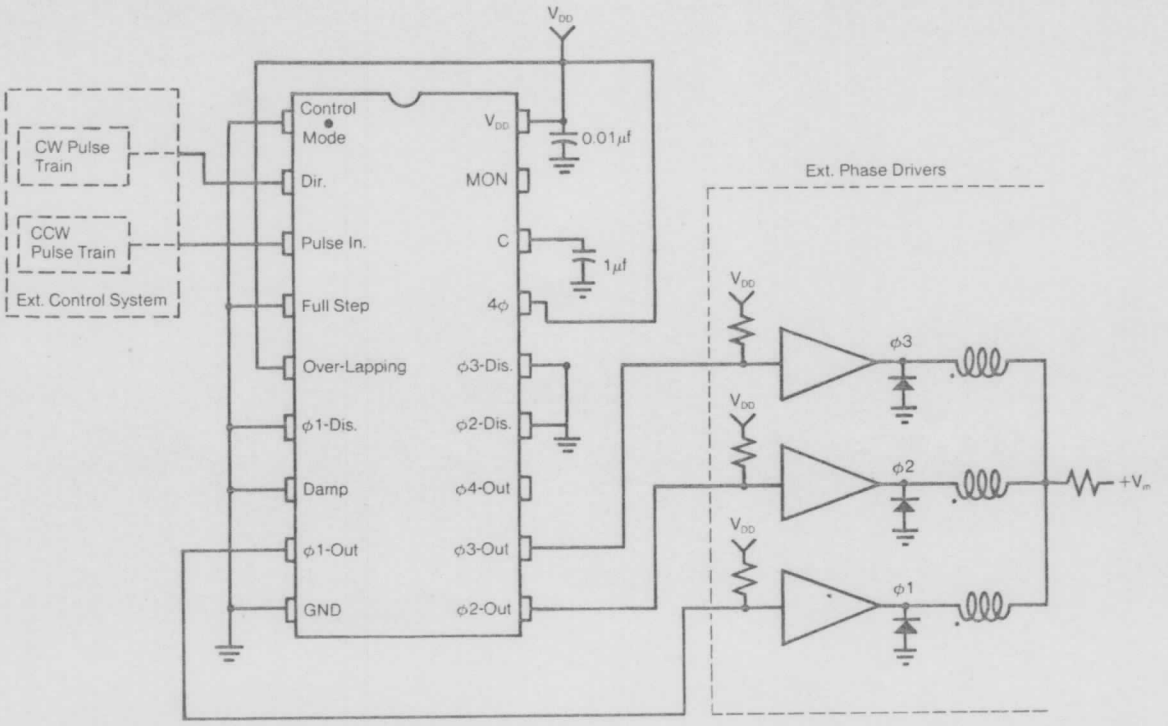


Fig. 4.5 Connections for Three Phase, Full Step Drive with Over-Lapping Phase Currents

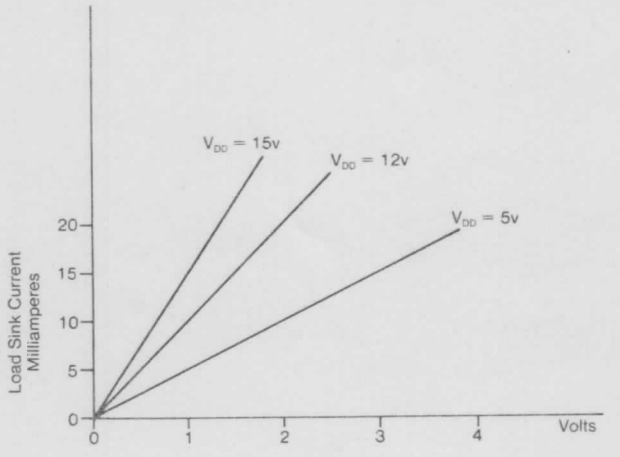


Fig. 4.6 Maximum Phase Output Saturation Voltage

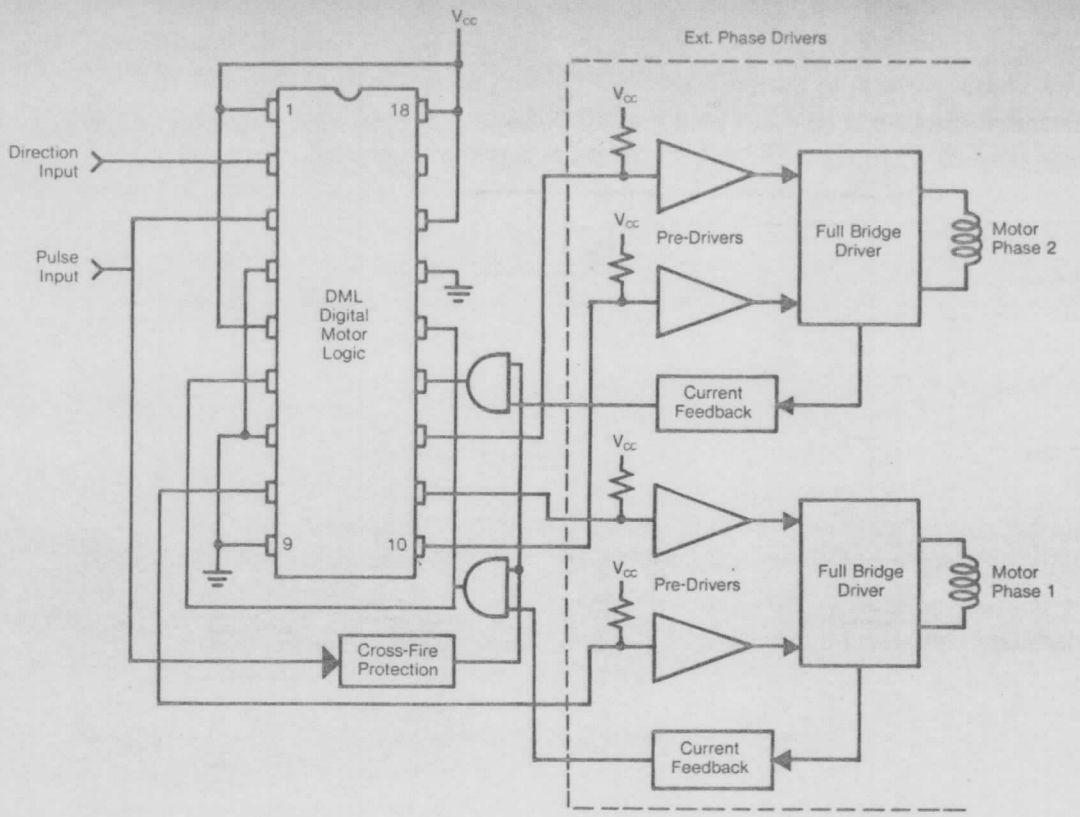


Fig. 4.7 Full Bridge, Current-Regulated Driver

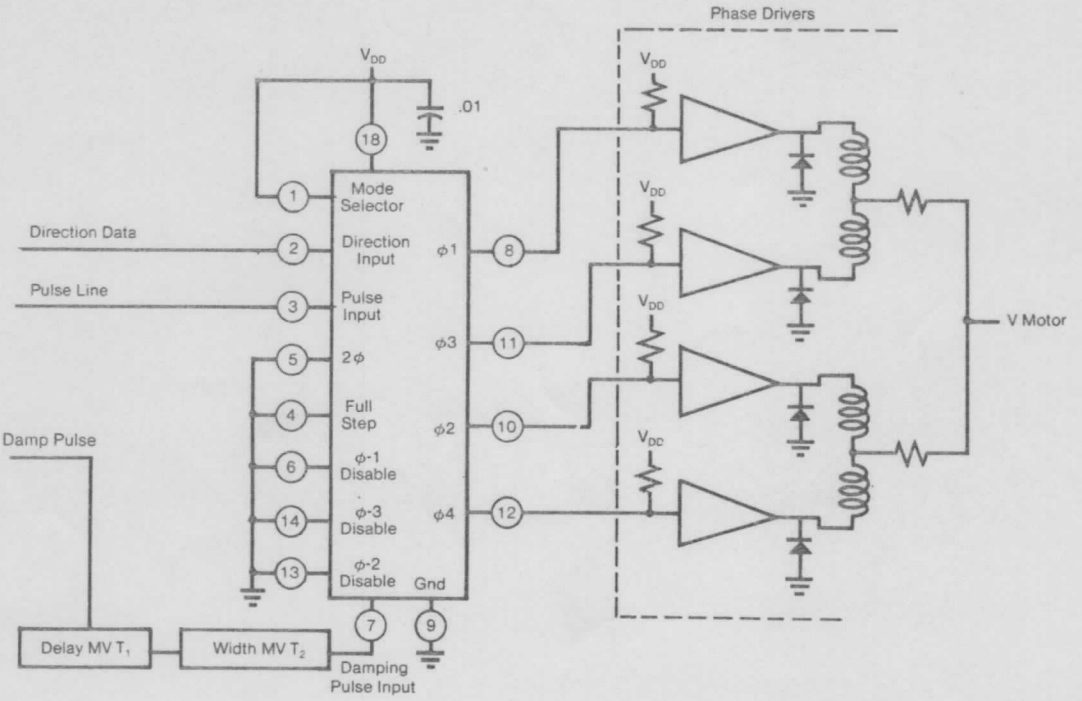
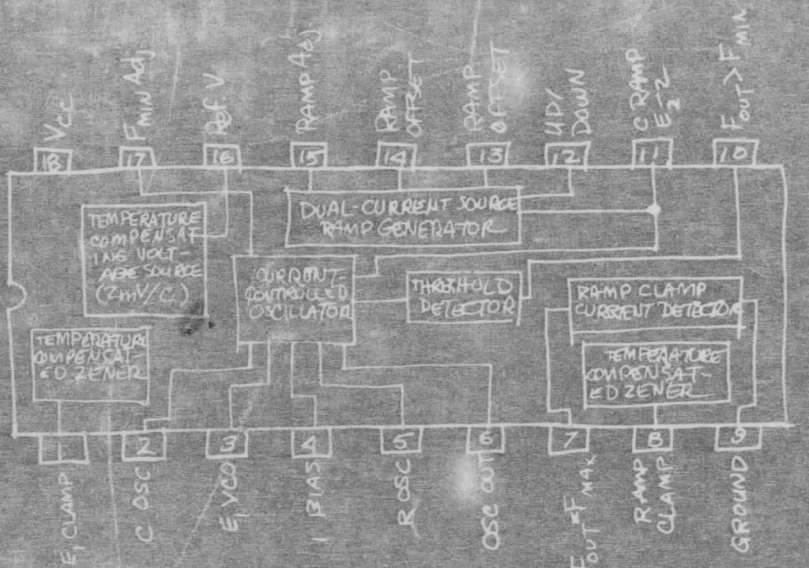
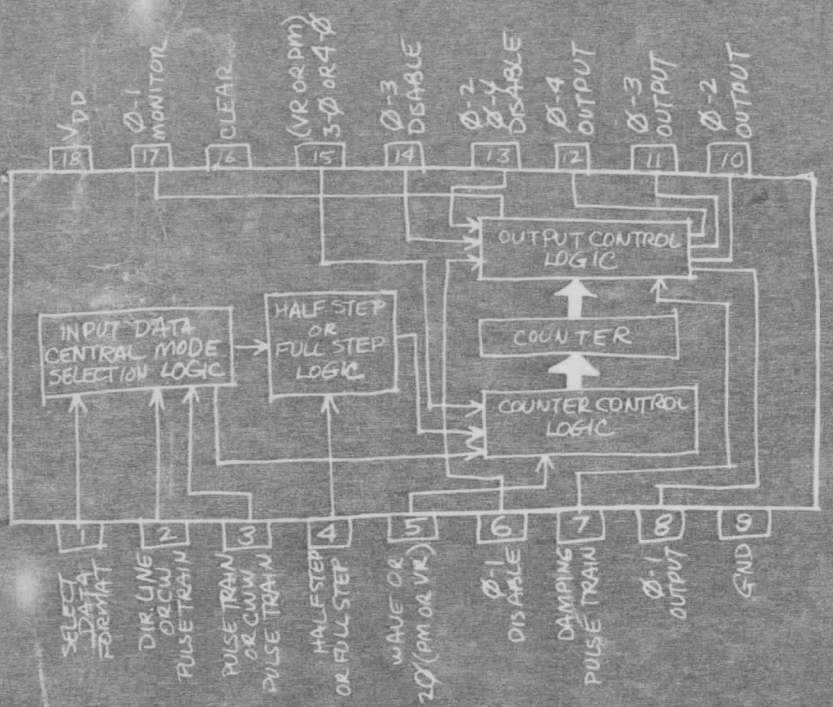
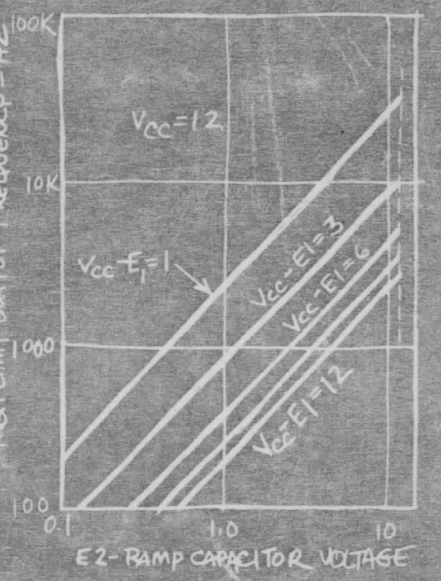


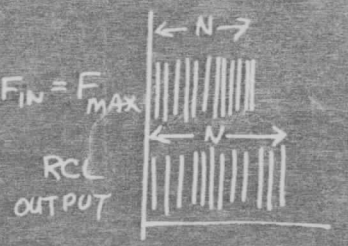
Fig. 4.8 Connection for Two-Phase, Full-Step Drive with Optional Reverse Pulse Damping

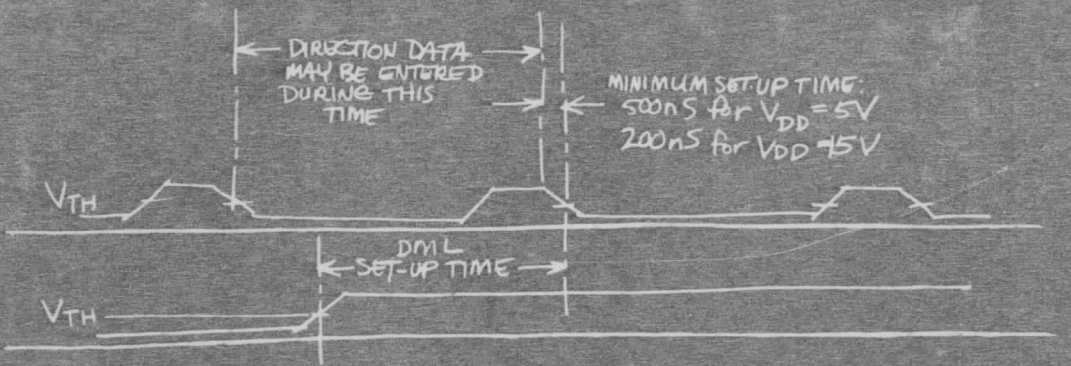
SIGMA stepping motor control chip set










DIRECTION DATA MAY BE ENTERED DURING THIS TIME
MINIMUM SET-UP TIME: 500nS for VDD = 5V 200nS for VDD = 15V
VTH
DIRL SET-UP TIME
VTH

The Sigma Stepping Motor Control Chip Set consists of three separate MSI integrated circuits which may be used in a variety of ways to provide low-power signals for the control or actuation of stepping motor drive systems. The set is designed specifically to provide a compact hardware alternative to those control functions which require extensive software to duplicate. Further, those functions which often require adjustment, frequency and ramp slope, are performed in the analog domain to facilitate adjustment without reprogramming.

The chips are constructed using bi-polar and CMOS circuitry, utilizing both linear and digital techniques. The chip set is designed to operate from a single 8-to-15 volt power supply. The input signals are typical logic levels, whereas most output signals are open-drain active circuits for maximum noise immunity.

Functionally, two chips, the RCO and RCL chips, form a "buffered ramper" which provides a variable frequency pulse train to control the acceleration of a stepping motor from a fixed frequency burst of pulses. Pulses "put aside" during acceleration are "put back" during deceleration. Thus, smooth motor response is assured while *the number of pulses is preserved.*

Used alone, the RCO voltage controlled oscillator and ramp generator can be used in a number of ways to generate fixed or variable frequency pulse trains, including ramped frequency trains for speed control applications.

The third circuit, the DML chip, accepts a pulse train and decodes it to all commonly used stepping motor excitation formats: 2-3-4 phase, half-step, full-step – and further provides specialized damping schemes as well. This chip alone is the heart of a motor power driver.

Ramp Control Logic (RCL) Chip* (Order Part No. 29G01)

The Ramp Control Logic Chip is normally used in conjunction with the RCO chip. The two chips provide a method of providing a variable frequency pulse train to control the acceleration and deceleration of a stepping motor from a fixed frequency burst of pulses. The output of these chips can drive the DML Motor Logic Chip or most any other stepping motor driver. The two chips, the RCL Ramp Control Chip and the RCO Ramp Control Oscillator form a "Buffered Ramper". A buffered ramper accepts a constant high frequency pulse train and delivers a variable frequency output with preset acceleration and deceleration profiles.

VETTOA1

Figure 1 – Functional Block Diagram of RCL Module

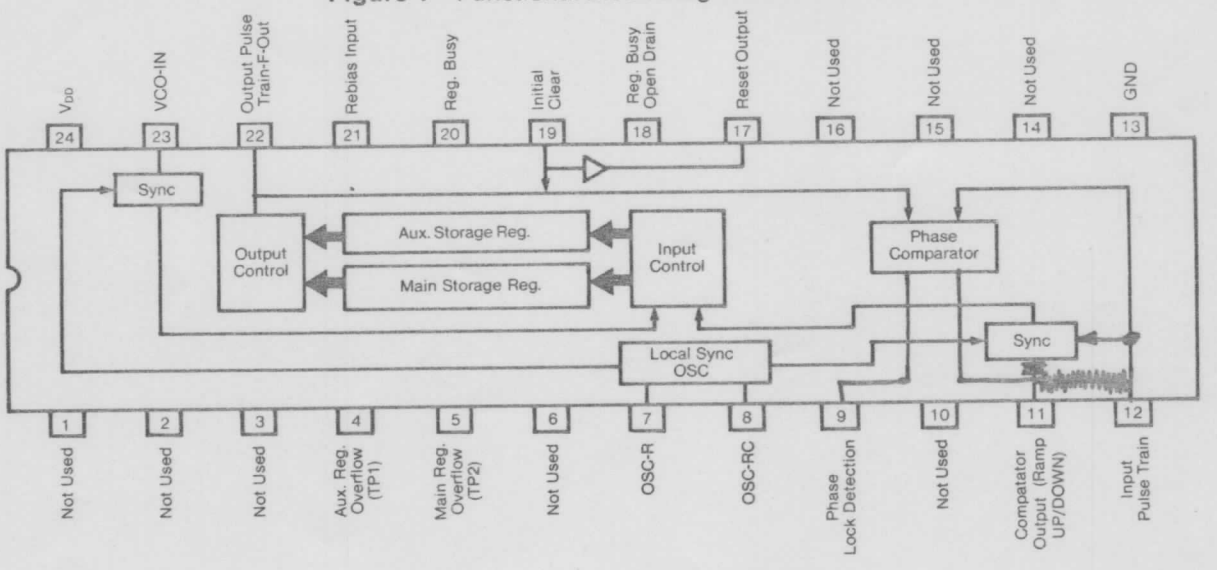
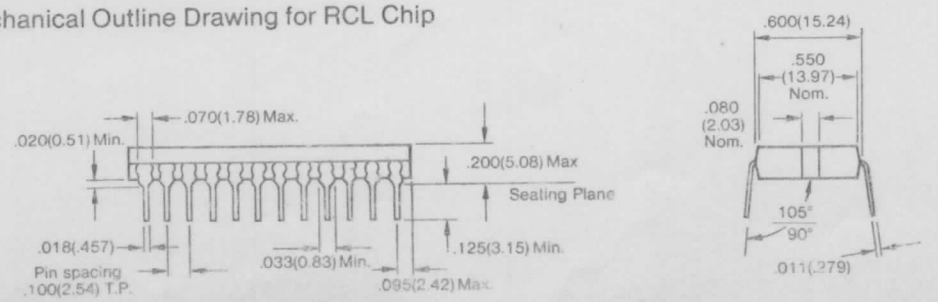


Figure 2 – Mechanical Outline Drawing for RCL Chip



*patent applied for

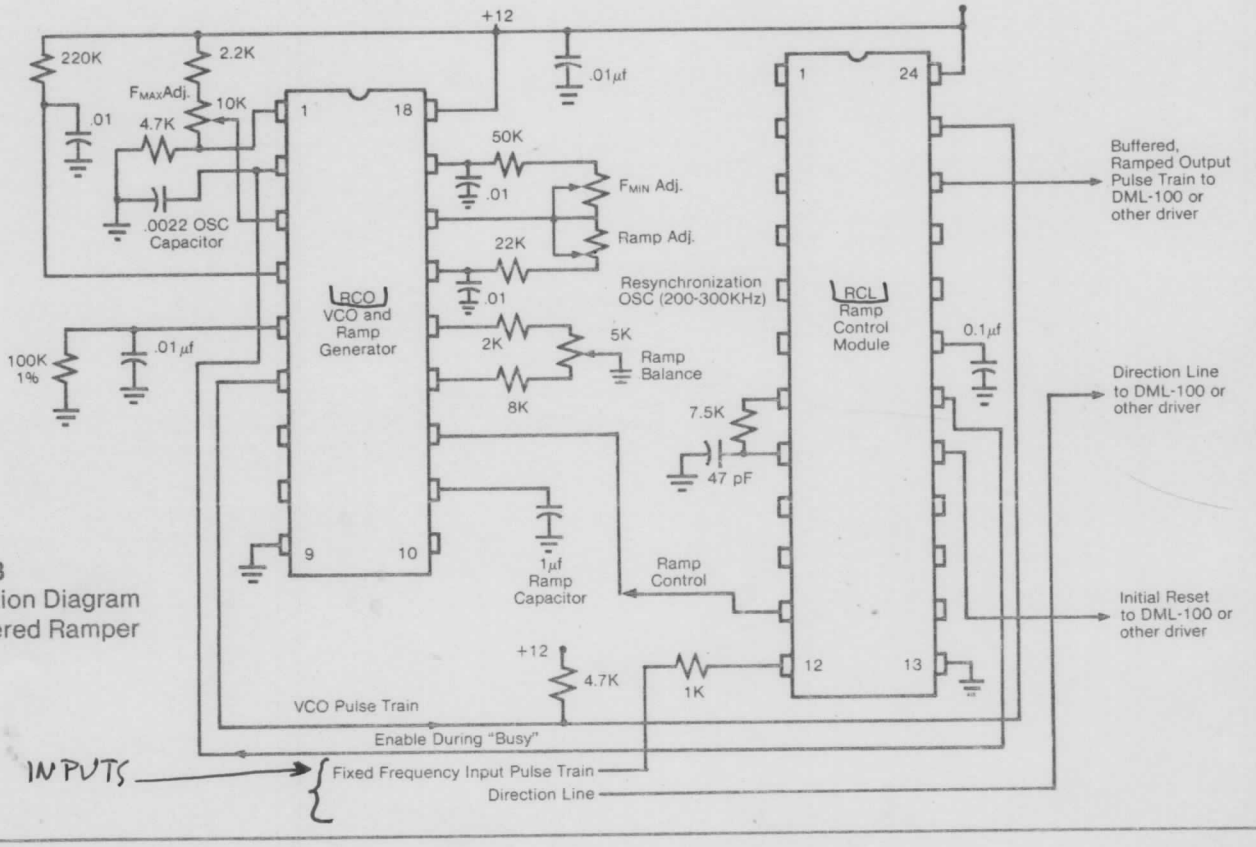


Figure 3
Connection Diagram for Buffered Ramper

Technical Data and Ratings

Maximum Ratings

Storage Temperature Range	−40 to +125°C	Supply Voltage V_{DD} to GND	16.5V
Operating Temperature Range	0 to +85°C	Package Power Dissipation	400mw

Operating Conditions at 25°C

Characteristic	Nominal	Min.	Max.	Units	
V_{DD}	12	8	15	V	± 10%
Supply Current	V_{DD} = 10V V_{DD} = 15V		0.5 1.0	mA	Built-in pull-up loads Logic inputs at GND
Input signal Voltage Range	0 to V_{DD}	0.2V_{DD} to 0.8V_{DD}	− 0.5V to V_{DD} + 0.5V	V	
Input Pulse Train Frequency			30	KHz	F_{IN} set to freq. equivalent to to max. desired speed of motor.
Pulse width		15		µS	
Reset Pulse width		5		µS	
VCO Pulse Width		1.5		µS	
Freq. Re-Sync OSC	750	600	1000	KHz	Depends on Ext. R-C value

Static Electrical Conditions at 25°C

Characteristic	V_{DD}	Conditions	Min.	Nominal	Max.	Units	Pins
Logic input Current	10 15	Inputs at Logic 0 (GND)		10 10		pA pA	F_{in} RC
Logic input Current	10 15	Inputs at Logic 0 (GND)		0.16 0.35	0.3 0.5	mA	F_{VCO}
Logic input Current	10 15	Inputs at Logic 0 (GND)		8 15	15 30	µA	C
Logic input Current		Inputs at Logic 1 (V_{DD})		10pA		pA	F_{IN}, F_{VCO} etc.
Buffered Logic output Current Sink rating	10 15	V_{SAT} =0.5V	10 1.5			mA	Comp Out F_{out}, R_o etc.
Open Drain Busy output Current Sink	10 15	Output Logic 0 V_{SAT} = 0.5V	1.0 1.5			mA	
Open Drain Busy Voltage Rating		Output at Logic 1 V_S = 20V			10	µA	V_S = 20V Max.
Buffered Logic output Current Source	10 15	V_{OUT} = V_{DD} − 1V	1.0 1.5			mA	

Ramp Control Oscillator (RCO) Chip (Order Part No. 29G21)

This linear bi-polar chip contains a precision Voltage Controlled Oscillator for V-to-F conversions, as well as highly stable, precision current sources for charging an external capacitor to generate stable symmetrical voltage ramps. These voltage ramps are used to generate ramped frequency outputs from the VCO section. This chip can be used in a number of ways in conjunction with stepping motors:

1. Phase-locked loop buffered ramper when used with the RCL chip.
2. Fixed or variable frequency source for simple speed control.
3. Ramped frequency source for speed control external control logic.
4. Parabolic response V-to-F converter ($F = KV^2$) for wide range frequency control.

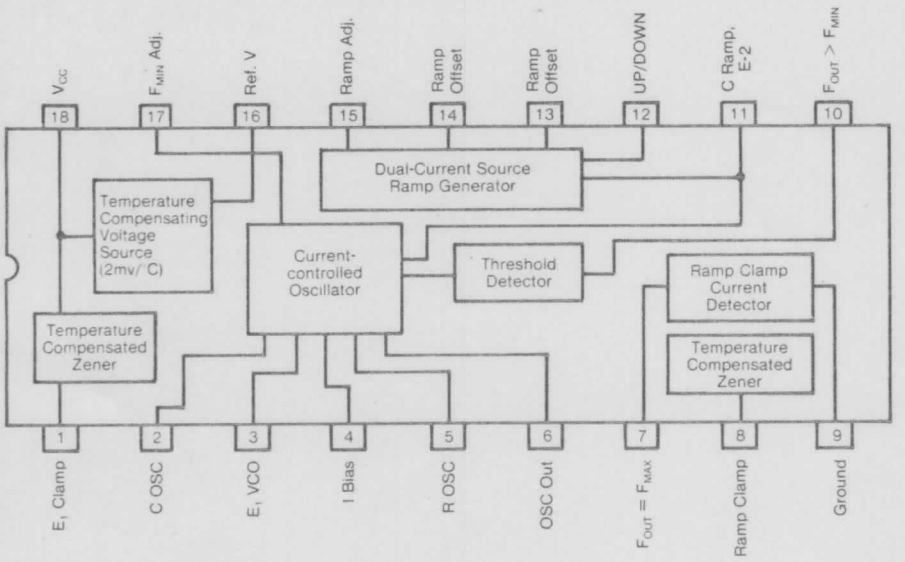


Figure 4 – Functional Block Diagram of RCO Chip

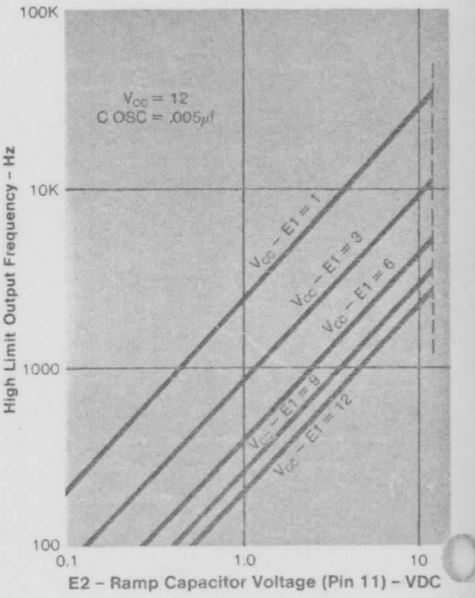


Figure 6
Oscillator Frequency Range

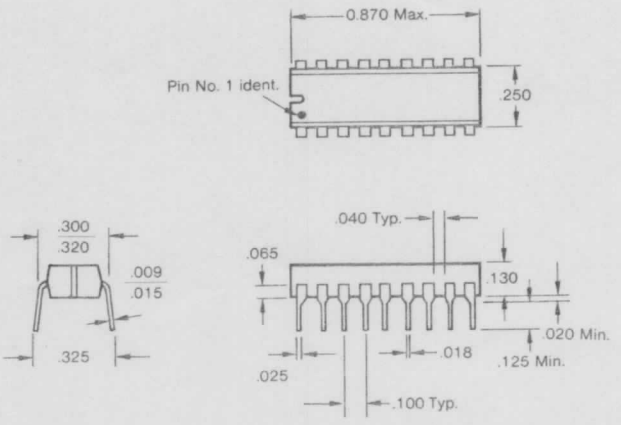


Figure 5 – Mechanical Outline Drawing for RCO Chip.

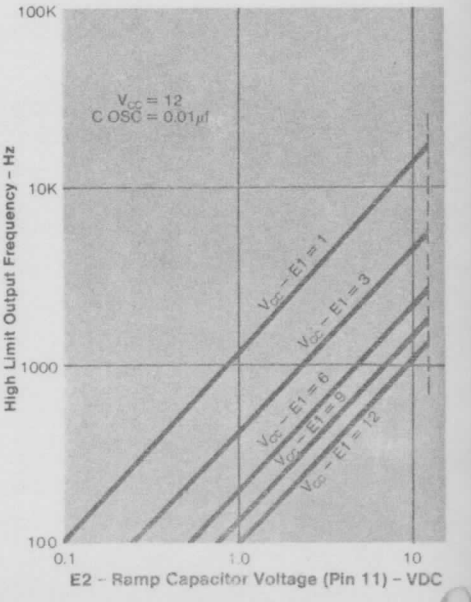
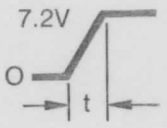


Figure 7
Oscillator Frequency Range

Ramp Time (t) vs. Resistance



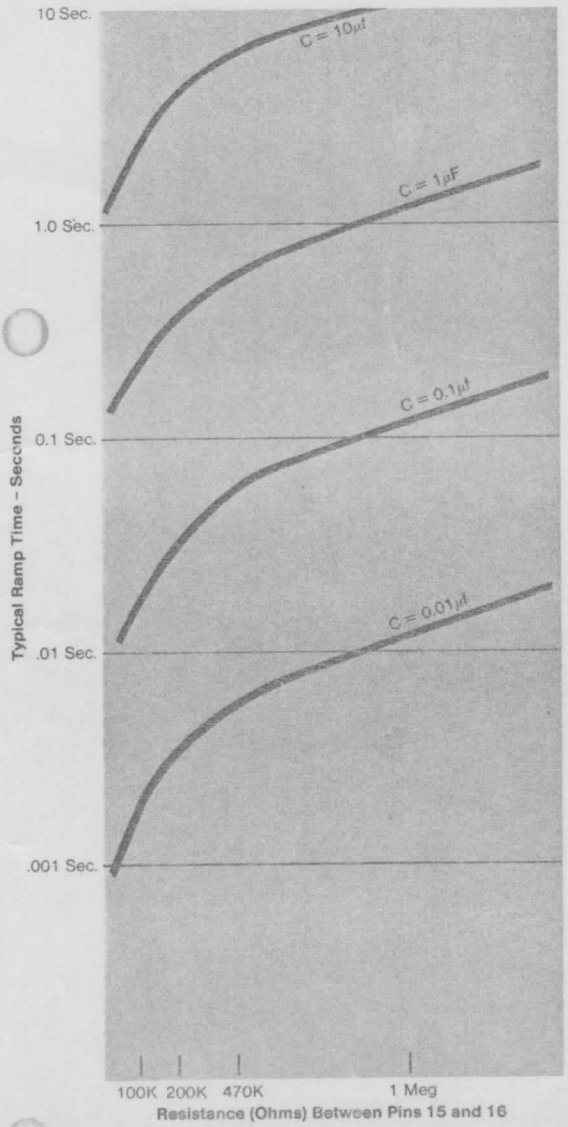


Figure 8

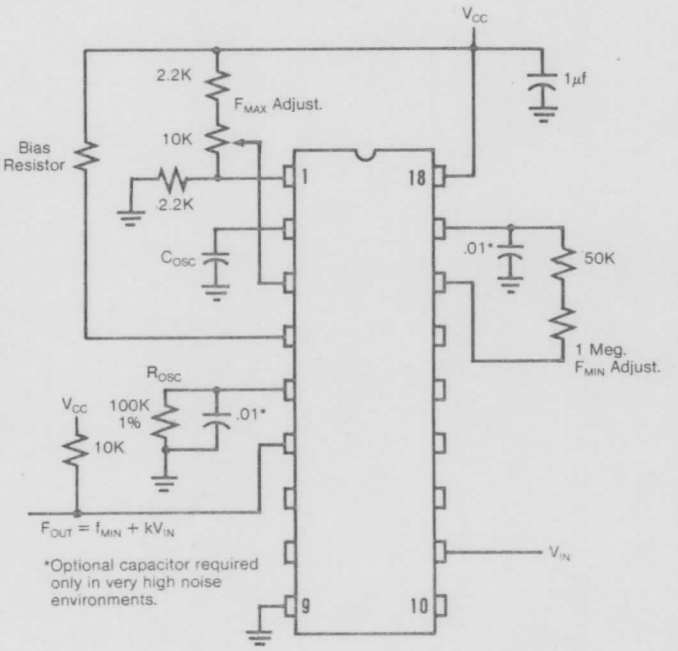


Figure 9 – Wide Range VCO with Linear Transfer Characteristics

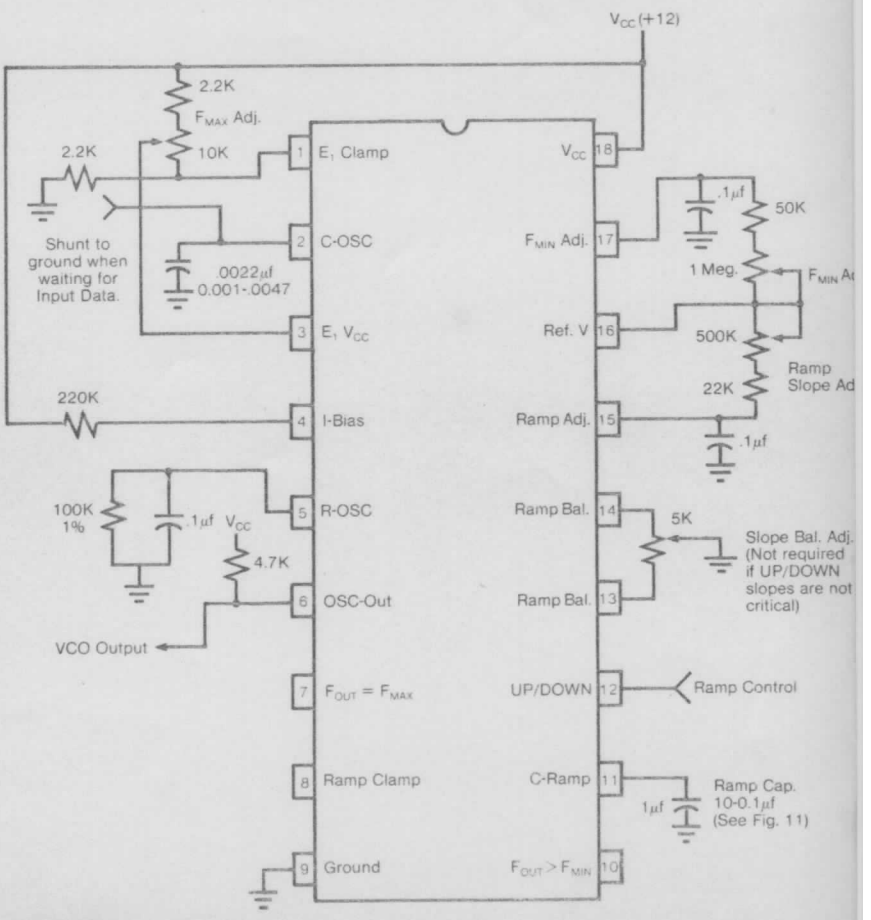


Figure 10 – Connections for Buffered Ramp Applications

Digital Motor Logic (DML) Chips (Order Part No. 29G41)

This CMOS logic chip accepts a pulse train input and decodes it into a selectable, parallel output stepping motor phase excitation format. The chip is the heart of a motor driver, generating the output states required at logic power levels. Sufficient flexibility is present in the chip to fit most data input and output formats. The input can be either dual pulse trains, CW or CCW, or a pulse line and a direction line.

The phase outputs can be two, three, or four phase in either the full step or half-step sequences. In addition, the outputs can be in wave or over-lapping sequences.

Further, the phase outputs can be selectively disabled for either standby power reduction or damping. There is a separate connection for a Reverse Pulse Damping input.

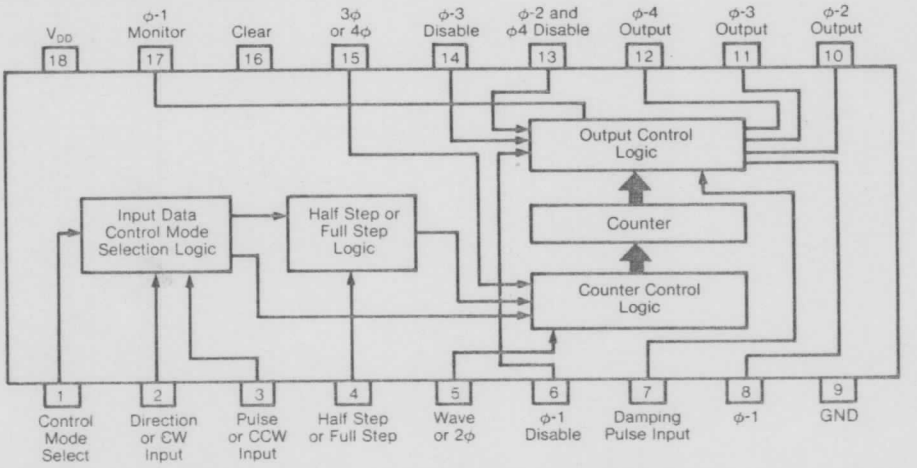


Figure 11
Functional Block Diagram of DML Chip

Figure 12 – Mechanical Outline Drawing for DML Chip and RCO Chip

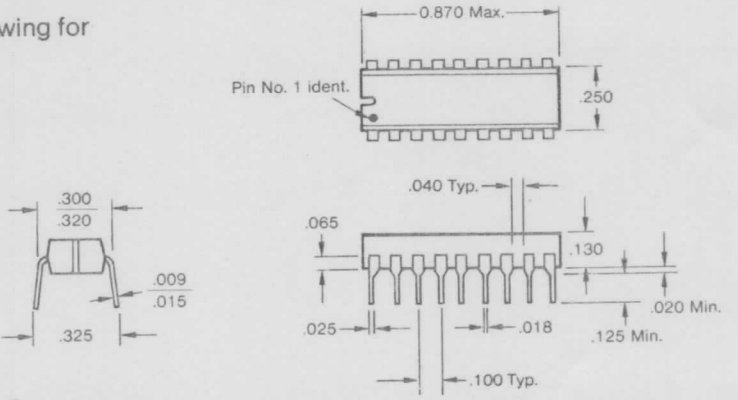
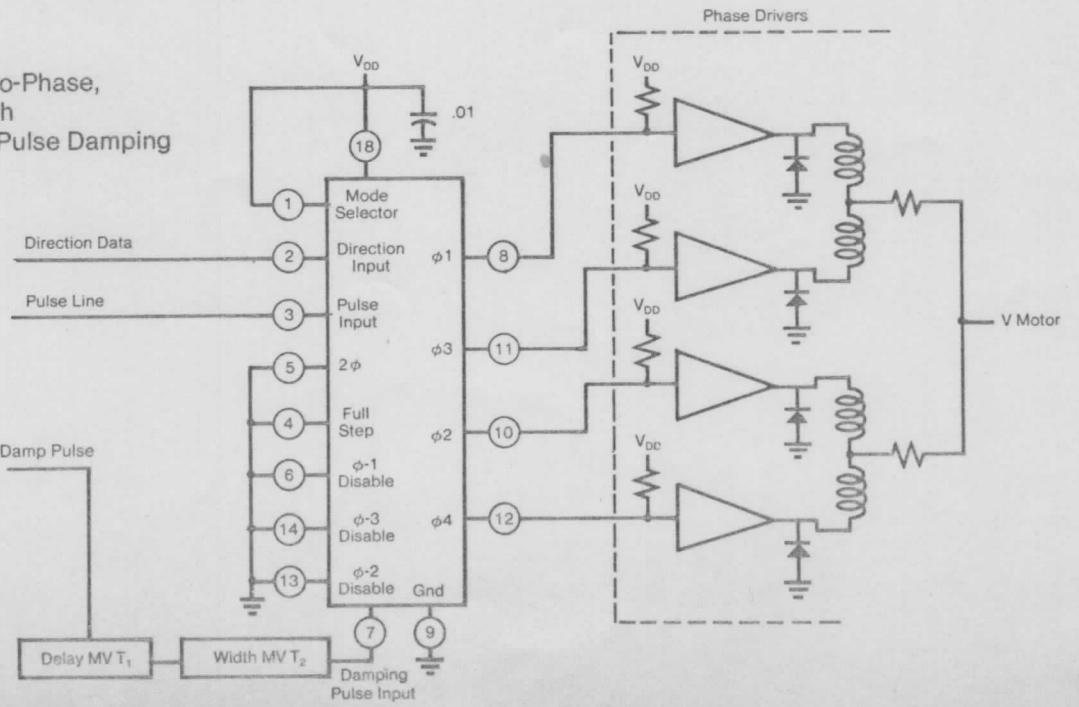


Figure 13
Connection for Two-Phase, Full-Step Drive with Optional Reverse Pulse Damping



TRUTH TABLE ONE

FULL STEP OUTPUT STATES

Pin 1 = 0 Pin 4 = 0 Pin 7 = 0 Pins 6, 13, 14 = 0

				Pin 5 = 0				Pin 5 = 1				
c/r	3φ/4φ	Dir/cw	Pulse/ccw	φ4	φ3	φ2	φ1	φ4	φ3	φ2	φ1	MON.
O	X	X	X	O	O	O	I	O	O	I	I	I
Three Phase States												
I	I	I	↓	O	O	I	O	O	I	I	O	O
I	I	I	↓	O	I	O	O	O	I	O	I	O
I	I	I	↓	O	O	O	I	O	O	I	I	I
I	I	O	↓	O	I	O	O	O	I	O	I	O
I	I	O	↓	O	O	I	O	O	I	I	O	O
I	I	O	↓	O	O	O	I	O	O	I	I	I
Two Phase States												
I	O	I	↓	O	O	I	O	O	I	I	O+	O
I	O	I	↓	O	I	O	O	I	I	O	O+	O
I	O	I	↓	I	O	O	O	I	O	O	I+	O
I	O	I	↓	O	O	O	I	O	O	I	I+	
I	O	O	↓	I	O	O	O	I	O	O	I+	O
I	O	O	↓	O	I	O	O	I	I	O	O+	O
I	O	O	↓	O	O	I	O	O	I	I	O+	O
I	O	O	↓	O	O	I	I	O	O	I	I+	I

O = Low level I = High level ↓High-to-low transition X = Don't care

+These states are commonly referred to as two-phase or also as four-phase drive. A four-phase motor is a center tapped two-phase motor.

TRUTH TABLE TWO

HALF STEP OUTPUT STATES

Pin 1 = 0 Pin 4 = 1 Pin 7 = 0 Pin 6, 13, 14 = 0 Pin 5 = X

c/r	3φ/4φ	Dir/cw	Pulse/ccw	φ4	φ3	φ2	φ1	MON.
O	X	X	X	O	O	O	I	I
Two Phase States								
I	O	I	↓	O	O	I	I	O
I	O	I	↓	O	O	I	O	O
I	O	I	↓	O	I	I	O	O
I	O	I	↓	O	I	O	O	O
I	O	I	↓	I	I	O	O	O
I	O	I	↓	I	O	O	O	O
I	O	I	↓	I	O	O	I	O
I	O	I	↓	O	O	O	I	I
I	O	O	↓	I	O	O	I	O
I	O	O	↓	I	O	O	O	O
I	O	O	↓	I	I	O	O	O
I	O	O	↓	O	I	O	O	O
I	O	O	↓	O	I	I	O	O
I	O	O	↓	O	O	I	O	O
I	O	O	↓	O	O	I	I	O
I	O	O	↓	O	O	O	I	I

c/r	3φ/4φ	Dir/cw	Pulse/ccw	φ4	φ3	φ2	φ1	MON.
O	X	X	X	O	O	O	I	I
Three Phase States								
I	I	I	↓	O	O	I	I	O
I	I	I	↓	O	O	I	O	O
I	I	I	↓	O	I	I	O	O
I	I	I	↓	O	I	O	O	O
I	I	I	↓	O	I	O	I	O
I	I	I	↓	O	O	O	I	I
I	I	O	↓	O	I	O	I	O
I	I	O	↓	O	I	O	O	O
I	I	O	↓	O	I	I	O	O
I	I	O	↓	O	O	I	O	O
I	I	O	↓	O	O	I	I	O
I	I	O	↓	O	O	O	I	I

O = Low level I = High level
↓ = High-to-low transition X = Don't care

TRUTH TABLE THREE

INPUT DATA MODES

Function

PIN 1 = 0
(pulse train and direction lines)

PIN 2
Direction input
1 = cw
0 = ccw
See figure 14 for timing requirements relative to pulse train.

PIN 3
Pulse train input
Pattern changes on high-to-low transition.

PIN 1 = ⏚
(cw pulse train and ccw pulse train)

Pulse train causes cw rotation, change occurs on high-to-low transition.

Pulse train causes ccw rotation, change occurs on high-to-low transition.

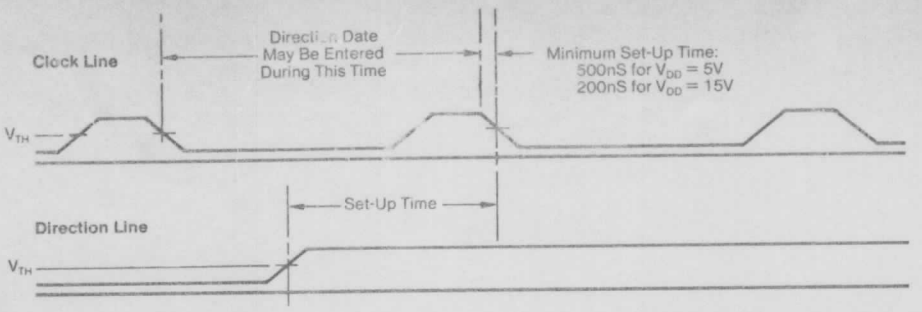

Clock Line
Direction Date May Be Entered During This Time
Minimum Set-Up Time: 500nS for V_{DD} = 5V 200nS for V_{DD} = 15V
V_{TH}
Set-Up Time
Direction Line
V_{TH}

Figure 14
Logic Module
Direction Line
Timing Requirements

Technical Data and Ratings

Maximum Ratings

Storage temperature range	−40 to +125°C	Phase output current sink capability	50mA
Operating temperature range	0 to + 85°C	Total package power dissipation+	400mW
Supply voltage V_{DD} to GND	16.5V		

+ derate at 100°C/watt to max junction temperature of 125°C

Operating Conditions at 25°C

Characteristic	Nominal	Min.	Max.	Units	
V_{DD} range	12	5	15	V	± 10%
Input voltage range	0 to V_{DD}	$0.2V_{DD}$ to $0.8V_{DD}$	−0.5V to V_{DD} +0.5V	V	
Pulse freq.		DC	200	KHz	KHz
Pulse width		2.5	None	μS	
Reset pulse width		5	None	μS	
Damping P.W.		5	None	μS	Motor + Sys. Dependent
Phase Dis. P.W.		5	None	μS	Motor + Sys. Dependent
Damping pulse delay			50	μS	
Phase Dis. delay			50	μS	
Pulse input rise		None	10	μS	
Direction input Set-up time	V_{DD} = 5V V_{DD} = 15V	500 200	None None	μS μS	See Figure 14

Static Electrical Conditions at 25°C

Characteristic	V_{DD}		Min	Nom	Max	Units	
Static Device Supply Current	5V 10V 15V	All-inputs Logic 0 (GND)		4 10 20	5 15 30	mA	Built pull-up loads
Logic input current	5V 10V 15V	All inputs logic 0 (GND)		.4 1.1 2.0	.6 1.6 2.5	μA	
Logic input current		All inputs logic V_{DD}			±100	nA	
Phase output voltage rating		Logic 1 out	20	35		V	
Phase output leakage current		Vs=20V			10	μA	
Phase output current sink capability	5V 10V 15V	Vsat= 1.0V	5 10 15			mA	
MON. output current sink capability	5V 10V 15V	Vo=0.5V	0.40 0.81 1.2			mA	
MON. output current source capability	5V 10V 15V	Vo=VOD −I.D.	0.5 1.0 1.5			mA	

SIGMA
MOTION CONTROL DIVISION
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